

Project Name :GM7MxxP

Platform : CFL-HR+N18E-GXR

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70. History

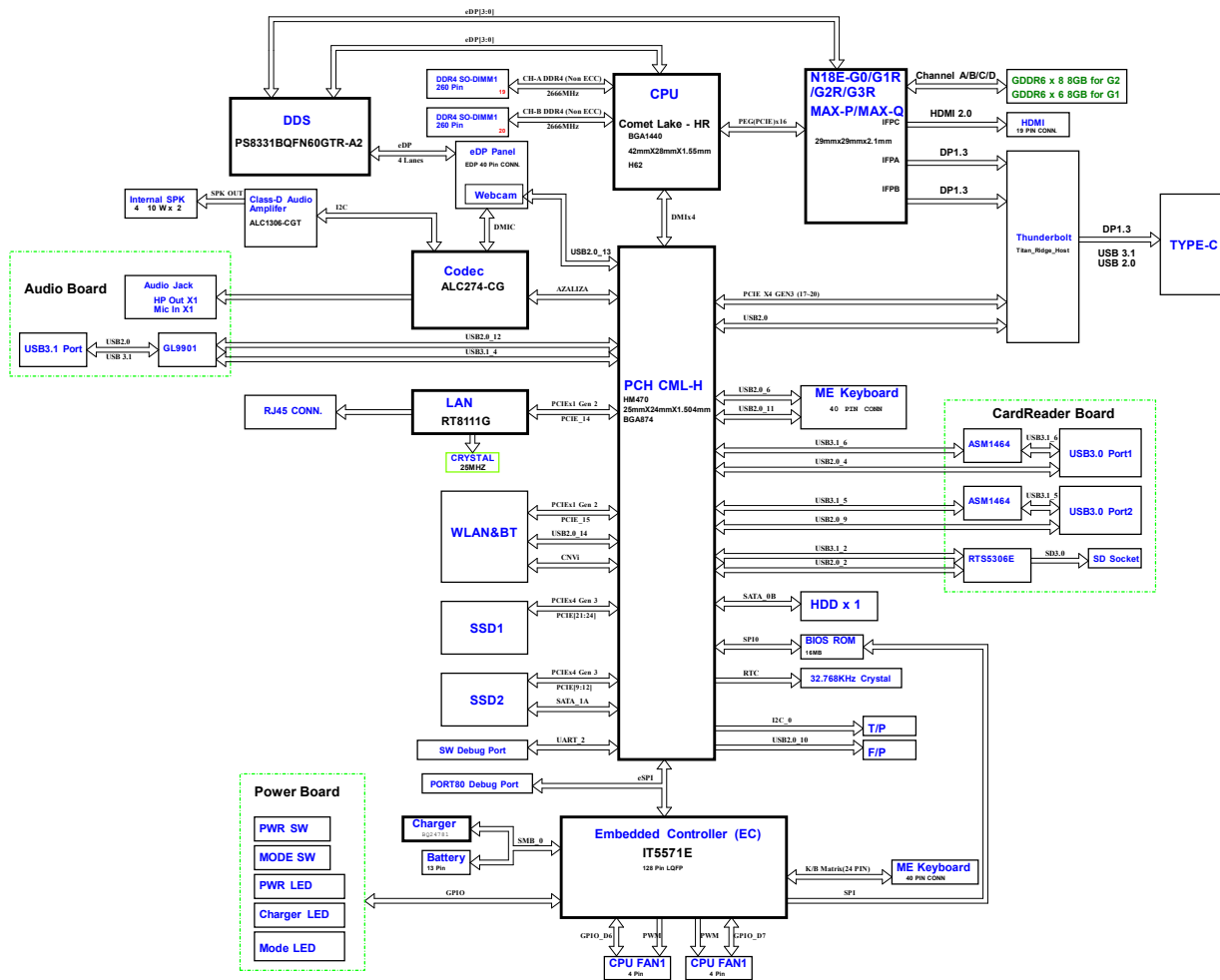
M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

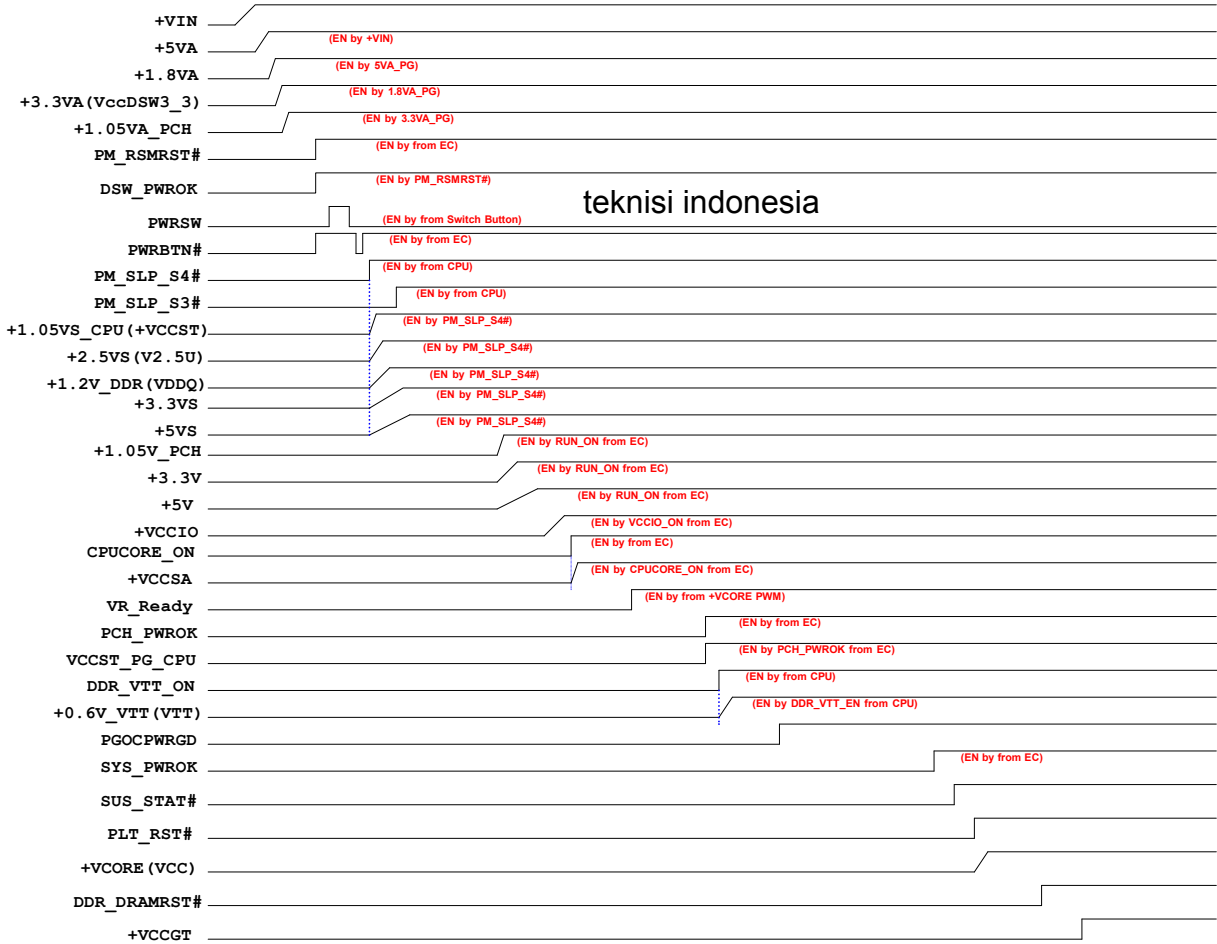
Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

SYSTEM BLOCK DIAGRAM

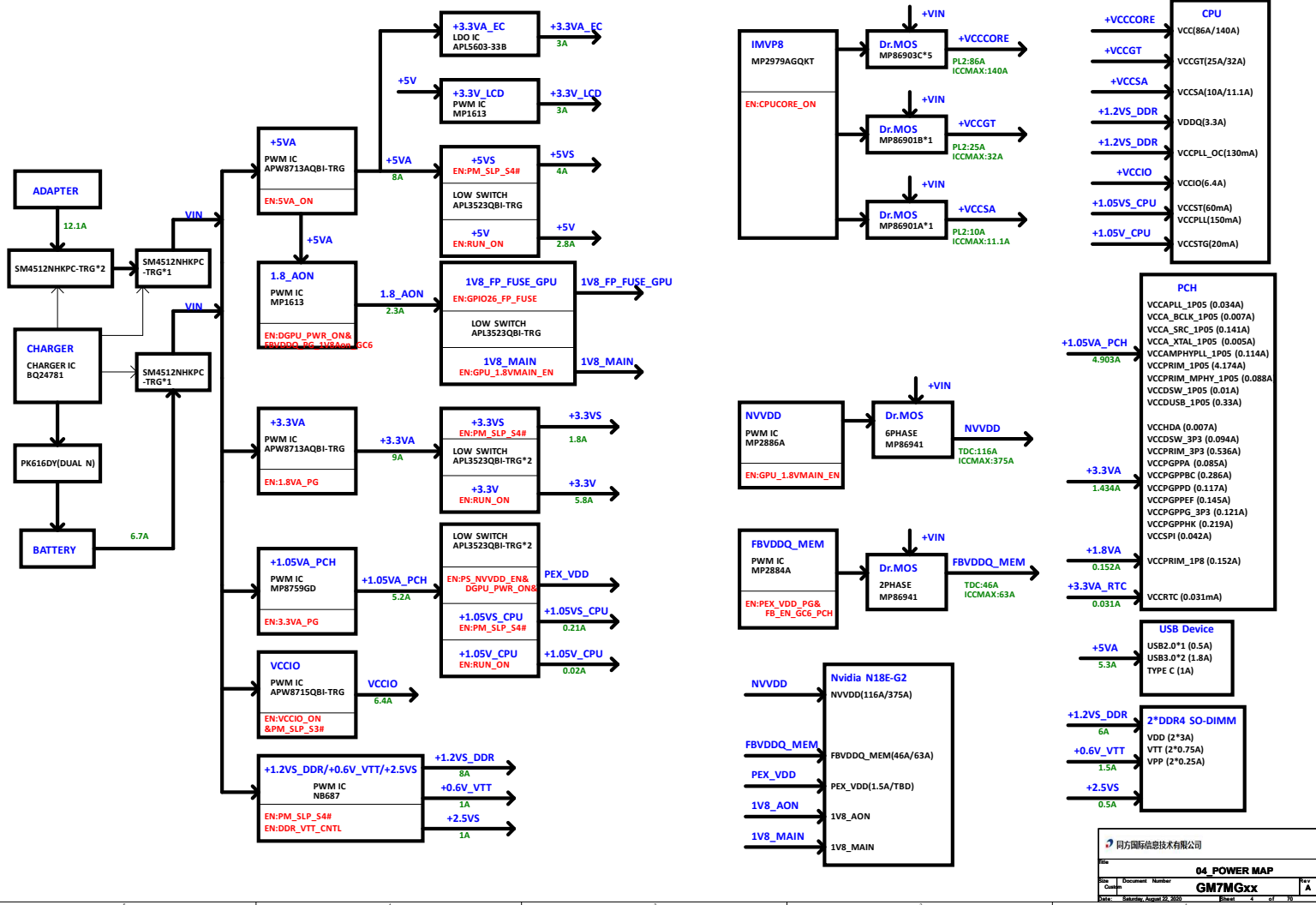


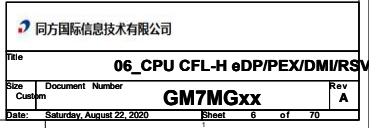
POWER ON SEQUENCE

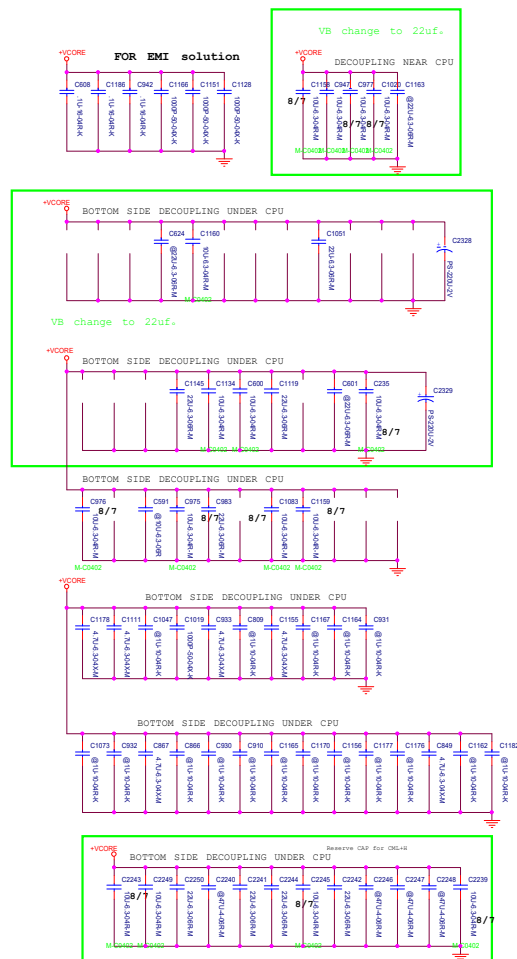
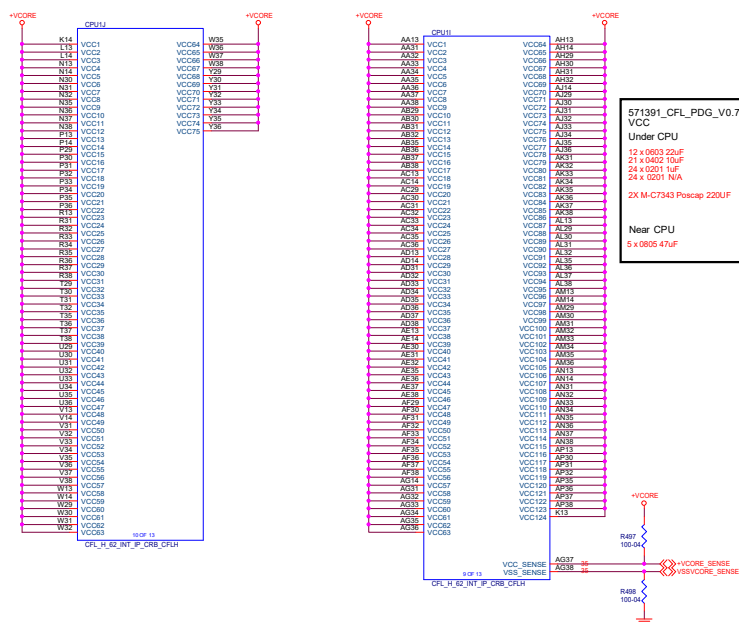


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611586_CML_H_PDG_Rev0p9
VccIO
Bulk Decoupling Example
Processor Decoupling Requirements

611586_CML_H_PDG_Rev0p9
VccSA
Bulk Decoupling Example
Processor Decoupling Requirements
2x 47uF 0805
2x 22uF 0603
7x 10uF 0402
1x 1uF 0201/0402

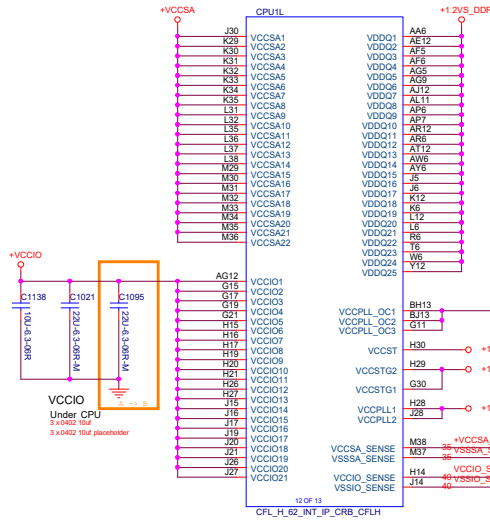
611586_CML_H_PDG_Rev0p9
Processor Decoupling Requirements
VDDQ
4x 22uF 0603
11x 10uF 0402
VccSTG
1x 1uF 0201/0402
VccPLL
1x 1uF 0201/0402
1x 22uF 0603
1x 22uF 0402
VccPLL_OC
2x 1uF 0201/0402

VccIO
Page 10 : 22u*2 + 10*1 = 54uF
Page 40 : 22u*4 = 88uF
Total : 142uF (CML-H spec : 124uF)

VccSA
Page 10 : 47u + 12 = 59uF
Page 36 : 22u + 4 = 26uF
Total : 85uF (spec : 523uF)

VDDQ
Page 10 : 22u * 15 = 330uF
Total : 330uF (spec : 198uF)

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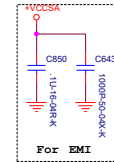
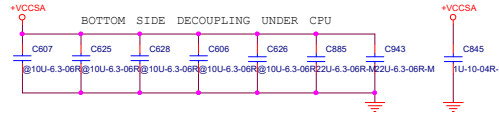
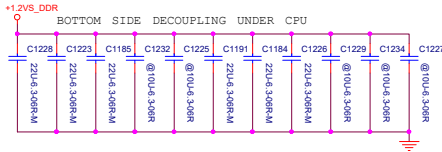
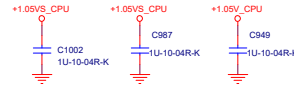
VCCST
Under CPU
1x 0201 1uF
VCCSTG
Under CPU
1x 0201 1uF
VCCPLL
Under CPU
1x 0201 1uF
VCCPLL_OC
Under CPU
2x 0201 1uF

VCCPLL_OC:
CPU digital PLL power rails
VCCPLL:
CPU PLL power rails

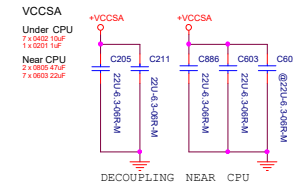
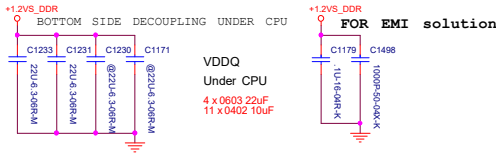
VCCSTG:
Sustain voltage for processor
in Standby modes
VCCSTG:
Gated version of VCCST

(1) VCCPLL is allowed to be OFF in S3,
but it is generally assumed to be ON
since it is powered from the same
source as VCCST.

(2) VCCPLL_OC is allowed to be turned
off during S3 if it is not powered
directly from VDDQ



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10_CPU CFL-H VCCSA/VCCIO/VDDQ			
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CPUIF			
A10	VSS_1	VSS_82	AK4
A12	VSS_3	VSS_84	AL10
A16	VSS_5	VSS_86	AL12
A18	VSS_7	VSS_88	AL14
A20	VSS_9	VSS_90	AL16
A22	VSS_11	VSS_92	AL18
A24	VSS_13	VSS_94	AL20
A26	VSS_15	VSS_96	AL22
A28	VSS_17	VSS_98	AL24
A30	VSS_19	VSS_100	AL26
A32	VSS_21	VSS_102	AL28
A34	VSS_23	VSS_104	AL30
A36	VSS_25	VSS_106	AL32
A38	VSS_27	VSS_108	AL34
A40	VSS_29	VSS_110	AL36
A42	VSS_31	VSS_112	AL38
A44	VSS_33	VSS_114	AL40
A46	VSS_35	VSS_116	AL42
A48	VSS_37	VSS_118	AL44
A50	VSS_39	VSS_120	AL46
A52	VSS_41	VSS_122	AL48
A54	VSS_43	VSS_124	AL50
A56	VSS_45	VSS_126	AL52
A58	VSS_47	VSS_128	AL54
A60	VSS_49	VSS_130	AL56
A62	VSS_51	VSS_132	AL58
A64	VSS_53	VSS_134	AL60
A66	VSS_55	VSS_136	AL62
A68	VSS_57	VSS_138	AL64
A70	VSS_59	VSS_140	AL66
A72	VSS_61	VSS_142	AL68
A74	VSS_63	VSS_144	AL70
A76	VSS_65	VSS_146	AL72
A78	VSS_67	VSS_148	AL74
A80	VSS_69	VSS_150	AL76
A82	VSS_71	VSS_152	AL78
A84	VSS_73	VSS_154	AL80
A86	VSS_75	VSS_156	AL82
A88	VSS_77	VSS_158	AL84
A90	VSS_79	VSS_160	AL86
A92	VSS_81	VSS_162	AL88
A94	VSS_83	VSS_164	AL90
A96	VSS_85	VSS_166	AL92
A98	VSS_87	VSS_168	AL94
A100	VSS_89	VSS_170	AL96
A102	VSS_91	VSS_172	AL98
A104	VSS_93	VSS_174	AL100
A106	VSS_95	VSS_176	AL102
A108	VSS_97	VSS_178	AL104
A110	VSS_99	VSS_180	AL106
A112	VSS_101	VSS_182	AL108
A114	VSS_103	VSS_184	AL110
A116	VSS_105	VSS_186	AL112
A118	VSS_107	VSS_188	AL114
A120	VSS_109	VSS_190	AL116
A122	VSS_111	VSS_192	AL118
A124	VSS_113	VSS_194	AL120
A126	VSS_115	VSS_196	AL122
A128	VSS_117	VSS_198	AL124
A130	VSS_119	VSS_200	AL126
A132	VSS_121	VSS_202	AL128
A134	VSS_123	VSS_204	AL130
A136	VSS_125	VSS_206	AL132
A138	VSS_127	VSS_208	AL134
A140	VSS_129	VSS_210	AL136
A142	VSS_131	VSS_212	AL138
A144	VSS_133	VSS_214	AL140
A146	VSS_135	VSS_216	AL142
A148	VSS_137	VSS_218	AL144
A150	VSS_139	VSS_220	AL146
A152	VSS_141	VSS_222	AL148
A154	VSS_143	VSS_224	AL150
A156	VSS_145	VSS_226	AL152
A158	VSS_147	VSS_228	AL154
A160	VSS_149	VSS_230	AL156
A162	VSS_151	VSS_232	AL158
A164	VSS_153	VSS_234	AL160
A166	VSS_155	VSS_236	AL162
A168	VSS_157	VSS_238	AL164
A170	VSS_159	VSS_240	AL166
A172	VSS_161	VSS_242	AL168
A174	VSS_163	VSS_244	AL170
A176	VSS_165	VSS_246	AL172
A178	VSS_167	VSS_248	AL174
A180	VSS_169	VSS_250	AL176
A182	VSS_171	VSS_252	AL178
A184	VSS_173	VSS_254	AL180
A186	VSS_175	VSS_256	AL182
A188	VSS_177	VSS_258	AL184
A190	VSS_179	VSS_260	AL186
A192	VSS_181	VSS_262	AL188
A194	VSS_183	VSS_264	AL190
A196	VSS_185	VSS_266	AL192
A198	VSS_187	VSS_268	AL194
A200	VSS_189	VSS_270	AL196
A202	VSS_191	VSS_272	AL198
A204	VSS_193	VSS_274	AL200
A206	VSS_195	VSS_276	AL202
A208	VSS_197	VSS_278	AL204
A210	VSS_199	VSS_280	AL206
A212	VSS_201	VSS_282	AL208
A214	VSS_203	VSS_284	AL210
A216	VSS_205	VSS_286	AL212
A218	VSS_207	VSS_288	AL214
A220	VSS_209	VSS_290	AL216
A222	VSS_211	VSS_292	AL218
A224	VSS_213	VSS_294	AL220
A226	VSS_215	VSS_296	AL222
A228	VSS_217	VSS_298	AL224
A230	VSS_219	VSS_300	AL226
A232	VSS_221	VSS_302	AL228
A234	VSS_223	VSS_304	AL230
A236	VSS_225	VSS_306	AL232
A238	VSS_227	VSS_308	AL234
A240	VSS_229	VSS_310	AL236
A242	VSS_231	VSS_312	AL238
A244	VSS_233	VSS_314	AL240
A246	VSS_235	VSS_316	AL242
A248	VSS_237	VSS_318	AL244
A250	VSS_239	VSS_320	AL246
A252	VSS_241	VSS_322	AL248
A254	VSS_243	VSS_324	AL250

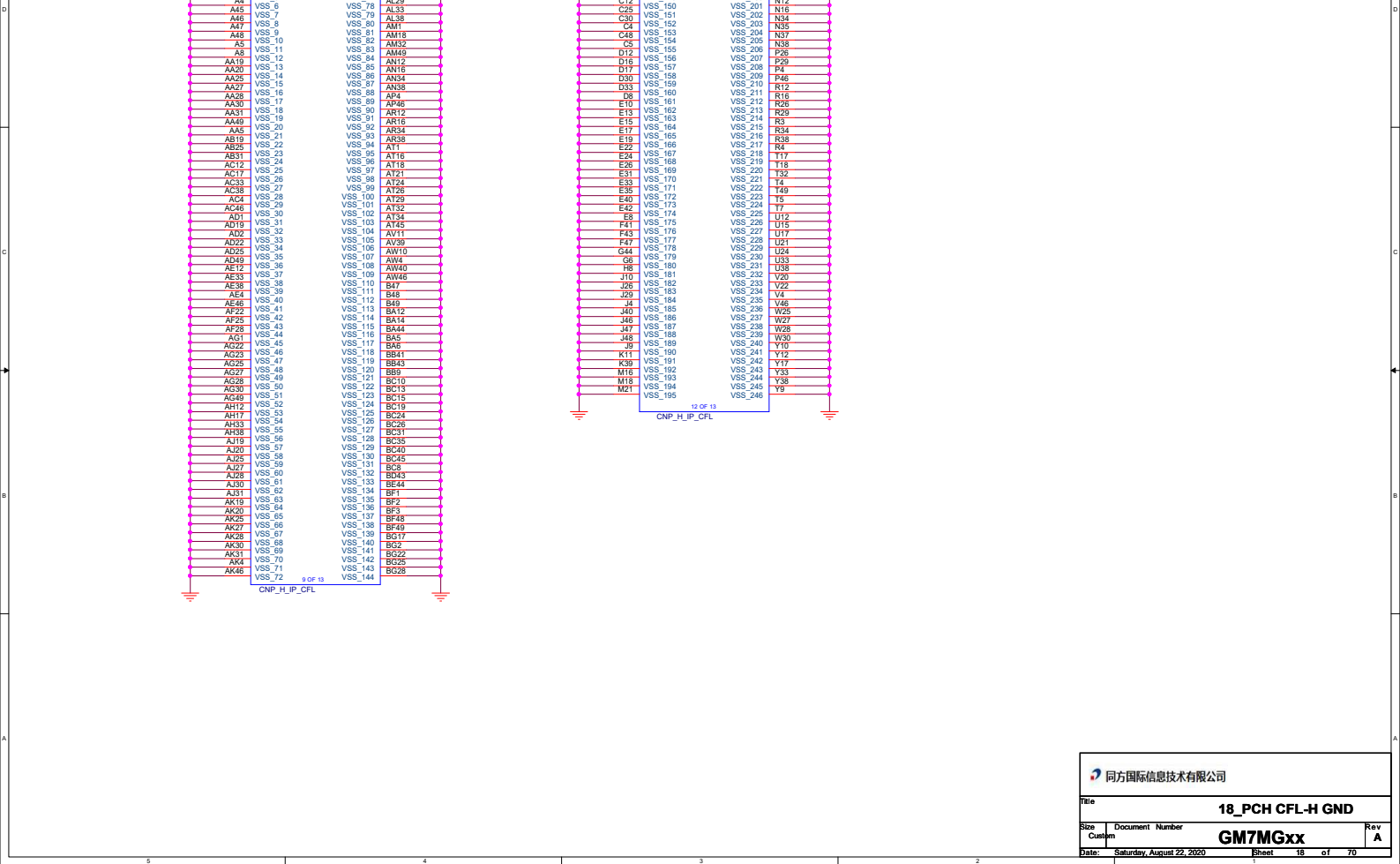
CPUIG			
AW5	VSS_163	VSS_244	BU15
AW7	VSS_165	VSS_246	BU17
AW9	VSS_167	VSS_248	BU19
AW11	VSS_169	VSS_250	BU21
AW13	VSS_171	VSS_252	BU23
AW15	VSS_173	VSS_254	BU25
AW17	VSS_175	VSS_256	BU27
AW19	VSS_177	VSS_258	BU29
AW21	VSS_179	VSS_260	BU31
AW23	VSS_181	VSS_262	BU33
AW25	VSS_183	VSS_264	BU35
AW27	VSS_185	VSS_266	BU37
AW29	VSS_187	VSS_268	BU39
AW31	VSS_189	VSS_270	BU41
AW33	VSS_191	VSS_272	BU43
AW35	VSS_193	VSS_274	BU45
AW37	VSS_195	VSS_276	BU47
AW39	VSS_197	VSS_278	BU49
AW41	VSS_199	VSS_280	BU51
AW43	VSS_201	VSS_282	BU53
AW45	VSS_203	VSS_284	BU55
AW47	VSS_205	VSS_286	BU57
AW49	VSS_207	VSS_288	BU59
AW51	VSS_209	VSS_290	BU61
AW53	VSS_211	VSS_292	BU63
AW55	VSS_213	VSS_294	BU65
AW57	VSS_215	VSS_296	BU67
AW59	VSS_217	VSS_298	BU69
AW61	VSS_219	VSS_300	BU71
AW63	VSS_221	VSS_302	BU73
AW65	VSS_223	VSS_304	BU75
AW67	VSS_225	VSS_306	BU77
AW69	VSS_227	VSS_308	BU79
AW71	VSS_229	VSS_310	BU81
AW73	VSS_231	VSS_312	BU83
AW75	VSS_233	VSS_314	BU85
AW77	VSS_235	VSS_316	BU87
AW79	VSS_237	VSS_318	BU89
AW81	VSS_239	VSS_320	BU91
AW83	VSS_241	VSS_322	BU93
AW85	VSS_243	VSS_324	BU95

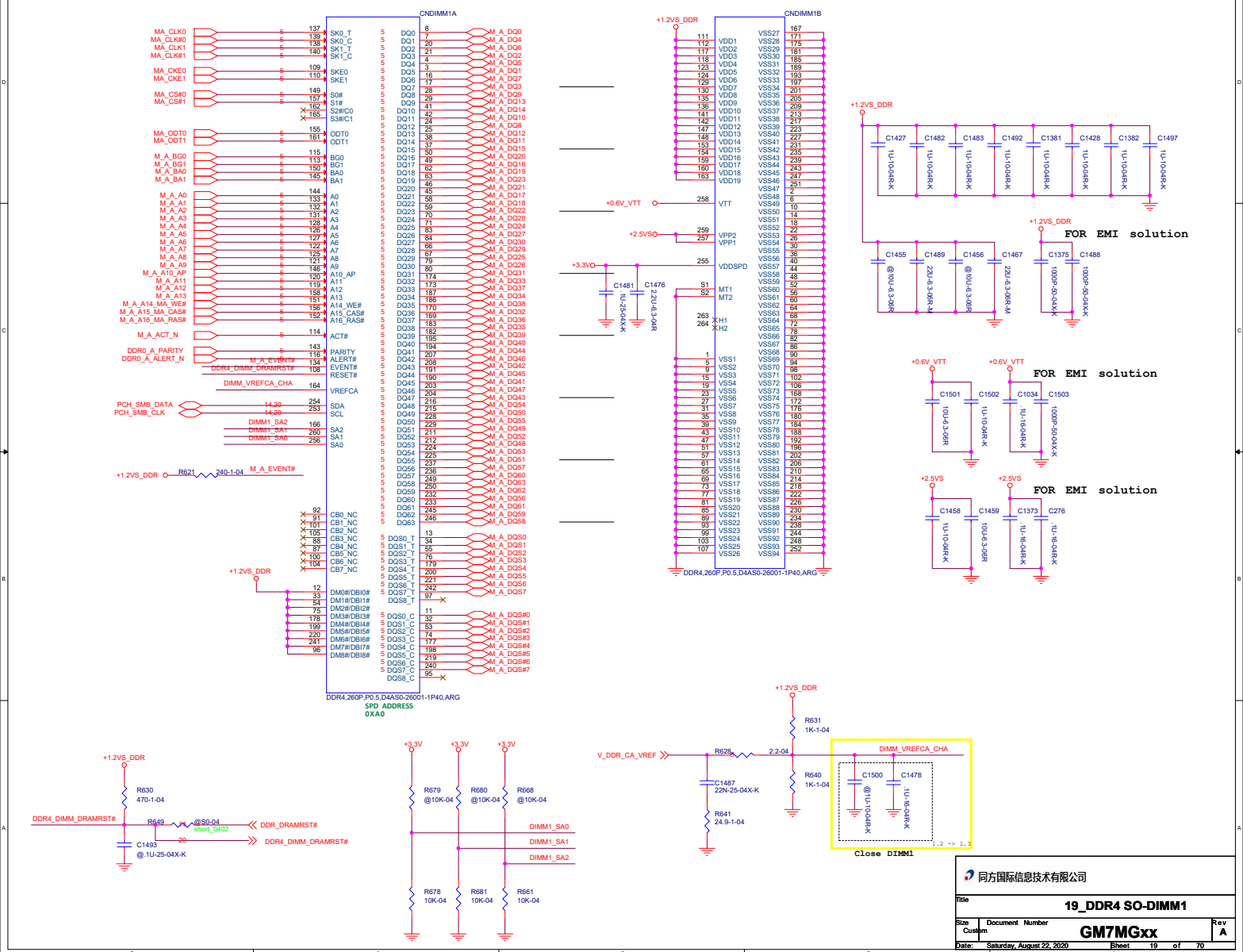
CPUIH			
BN4	VSS_325	VSS_409	F15
BN7	VSS_328	VSS_410	F17
BN12	VSS_327	VSS_411	F19
BN14	VSS_328	VSS_412	F21
BN18	VSS_329	VSS_413	F23
BN21	VSS_330	VSS_414	F25
BN25	VSS_331	VSS_415	F27
BN28	VSS_332	VSS_416	F29
BN29	VSS_333	VSS_417	F31
BN31	VSS_334	VSS_418	F33
BN33	VSS_335	VSS_419	F35
BN37	VSS_336	VSS_420	F37
BN42	VSS_337	VSS_421	F39
BN44	VSS_338	VSS_422	F41
BN48	VSS_339	VSS_423	F43
BN51	VSS_340	VSS_424	F45
BN54	VSS_341	VSS_425	F47
BN58	VSS_342	VSS_426	F49
BN62	VSS_343	VSS_427	F51
BN65	VSS_344	VSS_428	F53
BN68	VSS_345	VSS_429	F55
BN71	VSS_346	VSS_430	F57
BN74	VSS_347	VSS_431	F59
BN77	VSS_348	VSS_432	F61
BN81	VSS_349	VSS_433	F63
BN84	VSS_350	VSS_434	F65
BN87	VSS_351	VSS_435	F67
BN91	VSS_352	VSS_436	F69
BN94	VSS_353	VSS_437	F71
BN98	VSS_354	VSS_438	F73
BN101	VSS_355	VSS_439	F75
BN104	VSS_356	VSS_440	F77
BN108	VSS_357	VSS_441	F79
BN111	VSS_358	VSS_442	F81
BN114	VSS_359	VSS_443	F83
BN118	VSS_360	VSS_444	F85
BN121	VSS_361	VSS_445	F87
BN124	VSS_362	VSS_446	F89
BN127	VSS_363	VSS_447	F91
BN131	VSS_364	VSS_448	F93
BN134	VSS_365	VSS_449	F95
BN137	VSS_366	VSS_450	F97
BN141	VSS_367	VSS_451	F99
BN144	VSS_368	VSS_452	F101
BN147	VSS_369	VSS_453	F103
BN151	VSS_370	VSS_454	F105
BN154	VSS_371	VSS_455	F107
BN157	VSS_372	VSS_456	F109
BN161	VSS_373	VSS_457	F111
BN164	VSS_374	VSS_458	F113
BN167	VSS_375	VSS_459	F115
BN171	VSS_376	VSS_460	F117
BN174	VSS_377	VSS_461	F119
BN177	VSS_378	VSS_462	F121
BN181	VSS_379	VSS_463	F123
BN184	VSS_380	VSS_464	F125
BN187	VSS_381	VSS_465	F127
BN191	VSS_382	VSS_466	F129
BN194	VSS_383	VSS_467	F131
BN197	VSS_384	VSS_468	F133
BN201	VSS_385	VSS_469	F135
BN204	VSS_386	VSS_470	F137
BN207	VSS_387	VSS_471	F139
BN211	VSS_388	VSS_472	F141
BN214	VSS_389	VSS_473	F143
BN217	VSS_390	VSS_474	F145
BN221	VSS_391	VSS_475	F147
BN224	VSS_392	VSS_476	F149
BN227	VSS_393	VSS_477	F151
BN231	VSS_394	VSS_478	F153
BN234	VSS_395	VSS_479	F155
BN237	VSS_396	VSS_480	F157
BN241	VSS_397	VSS_481	F159
BN244	VSS_398	VSS_482	F161
BN247	VSS_399	VSS_483	F163
BN251	VSS_400	VSS_484	F165
BN254	VSS_401	VSS_485	F167
BN257	VSS_402	VSS_486	F169
BN261	VSS_403	VSS_487	F171
BN264	VSS_404	VSS_488	F173
BN267	VSS_405	VSS_489	F175
BN271	VSS_406	VSS_490	F177
BN274	VSS_407	VSS_491	F179
BN277	VSS_408	VSS_492	F181

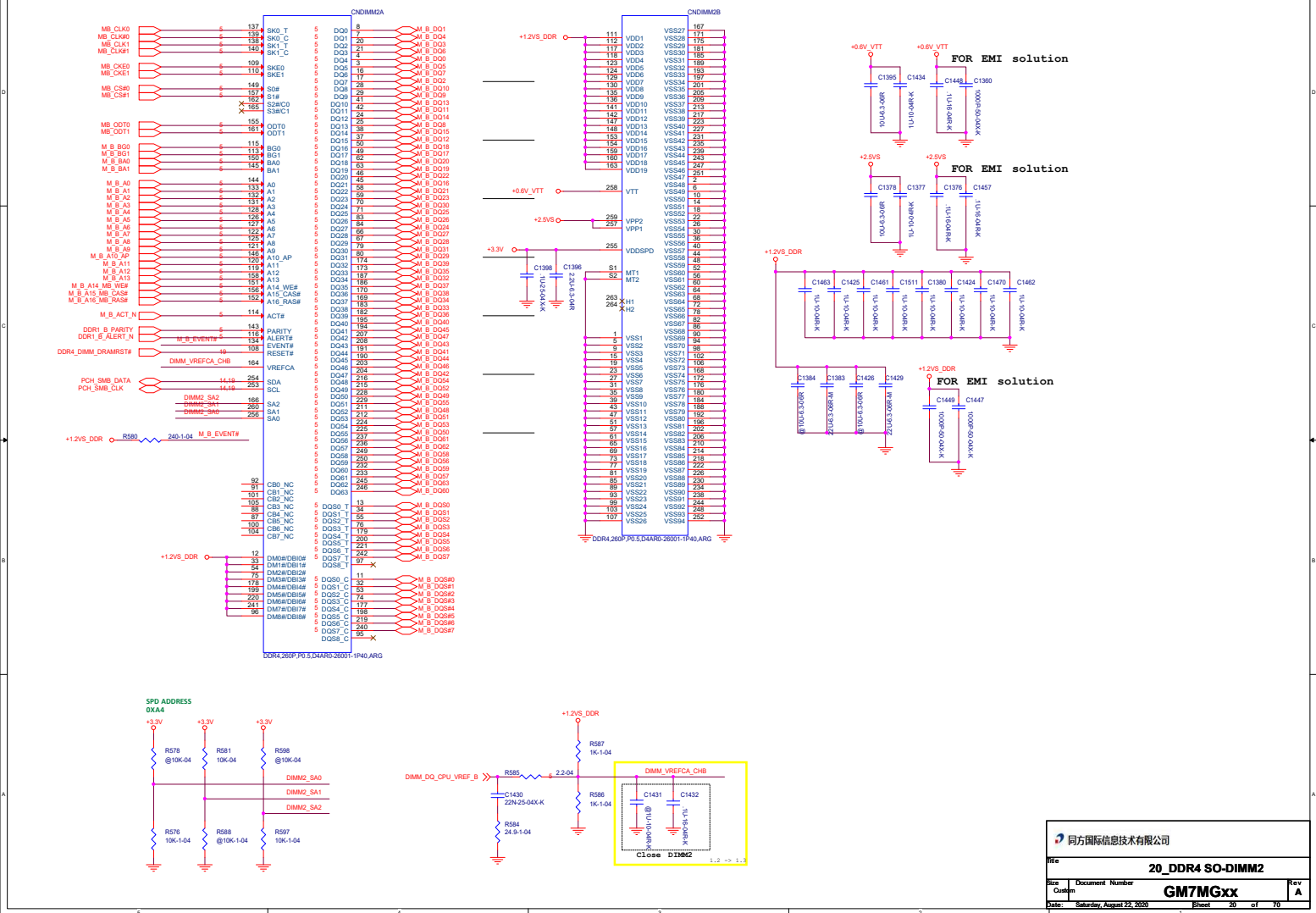


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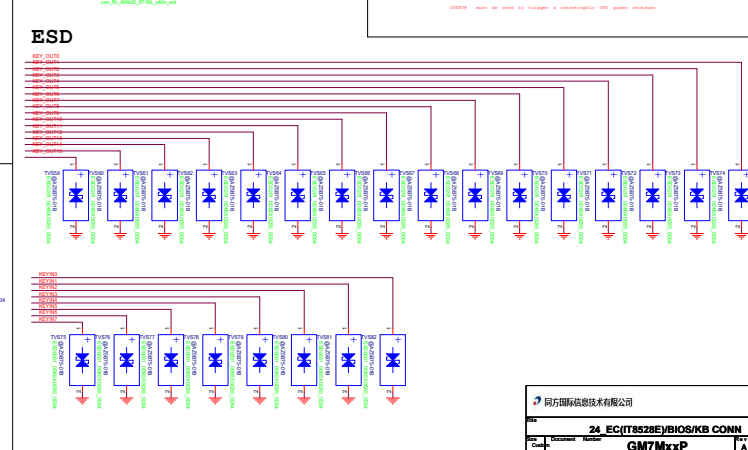
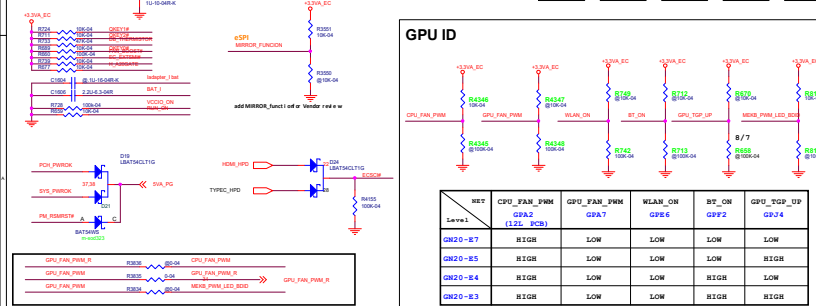
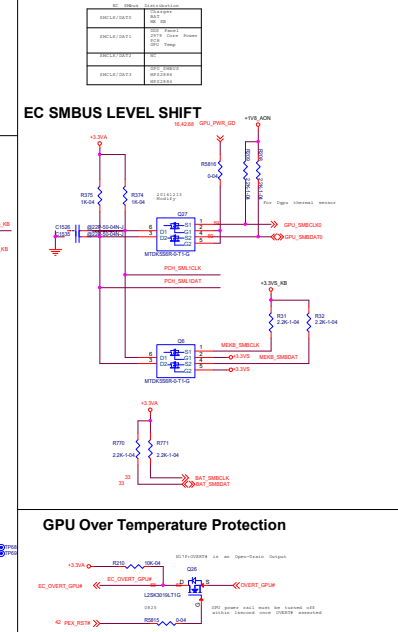
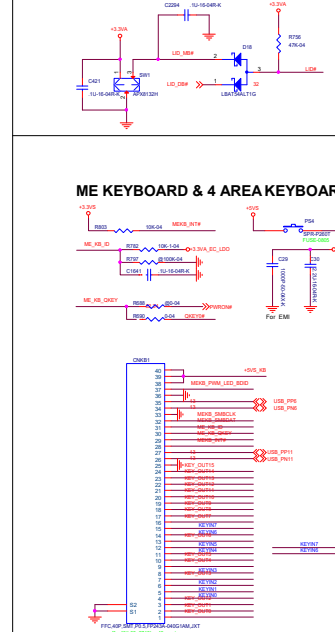
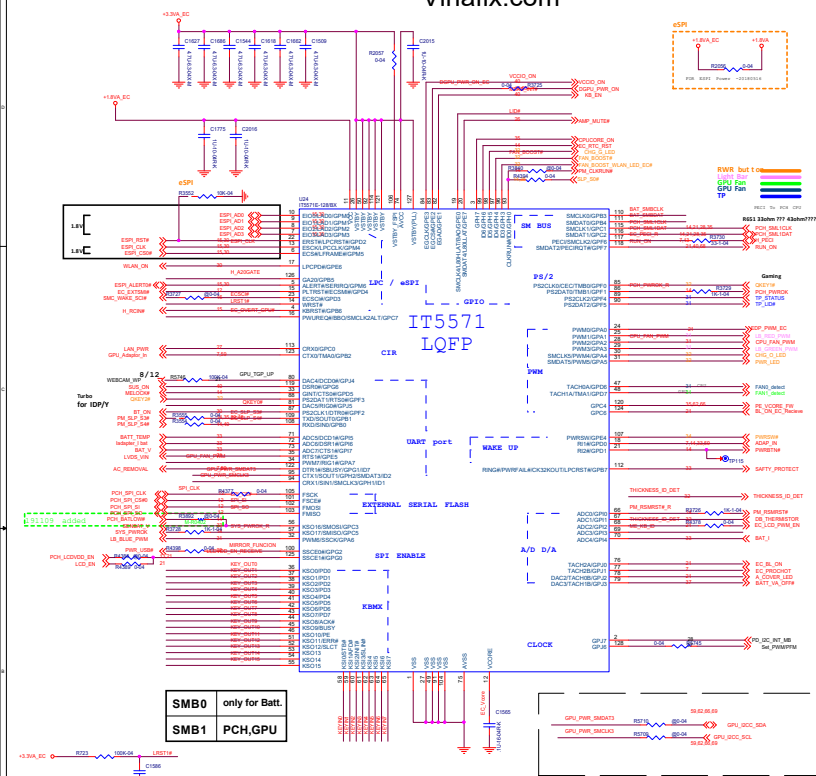








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Title			
23 Audio_Speaker Connector			
Rev	Document	Author	Rev
C		GM7MGxx	A
Date		Released	25 01 16



D

D

C

C

B

B

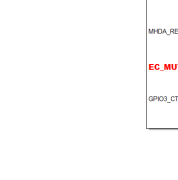
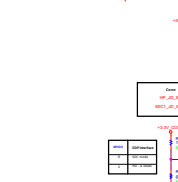
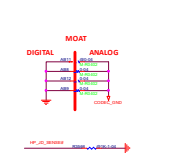
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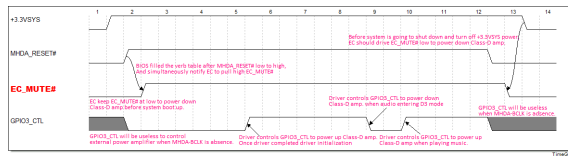
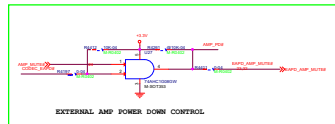
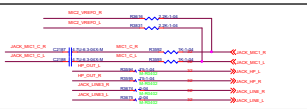
 同方国际信息技术有限公司			
Title		25 ME KB ESD	
Size A	Document Number		Rev A
Date: Saturday, August 22, 2020		Sheet 25 of 70	

CODEC-ALC274

NR
NR2
NR3
NR4

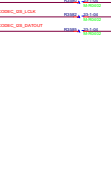
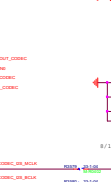


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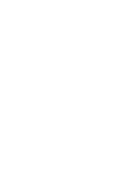
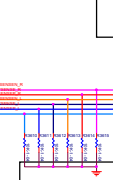
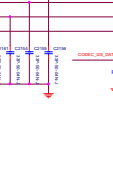
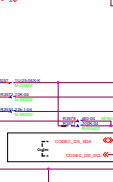
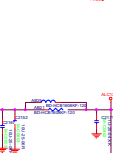


AMP-ALC1306

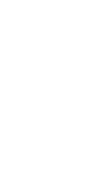
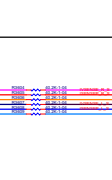
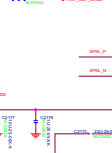
AMP-ALC1306



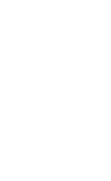
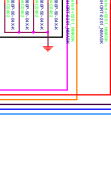
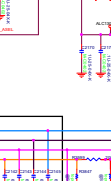
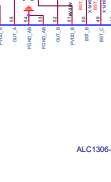
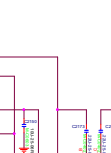
AMP-ALC1306



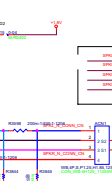
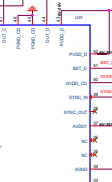
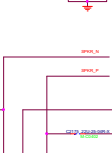
AMP-ALC1306



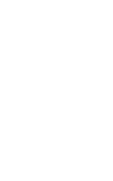
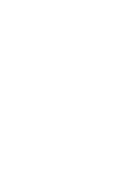
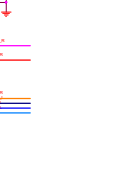
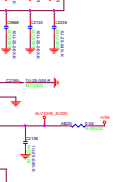
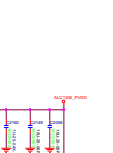
AMP-ALC1306



AMP-ALC1306



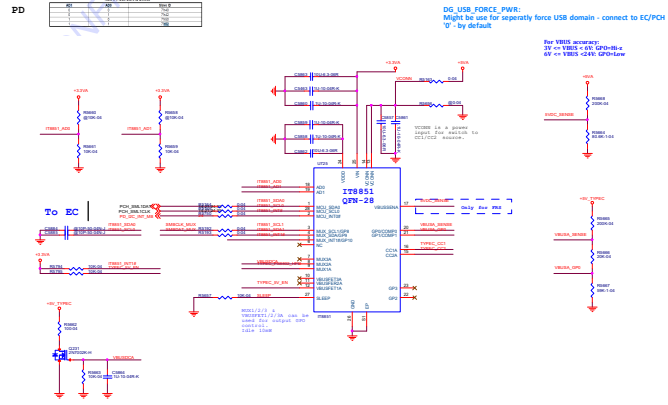
AMP-ALC1306



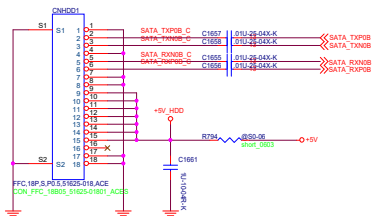
LAN



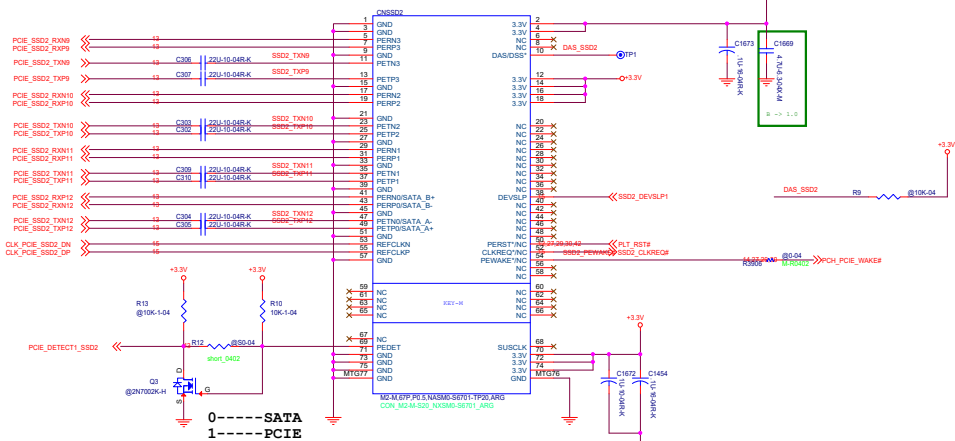
www.DeviceDB.XYZ - schematic, boardview, bios dump



SATA-HDD

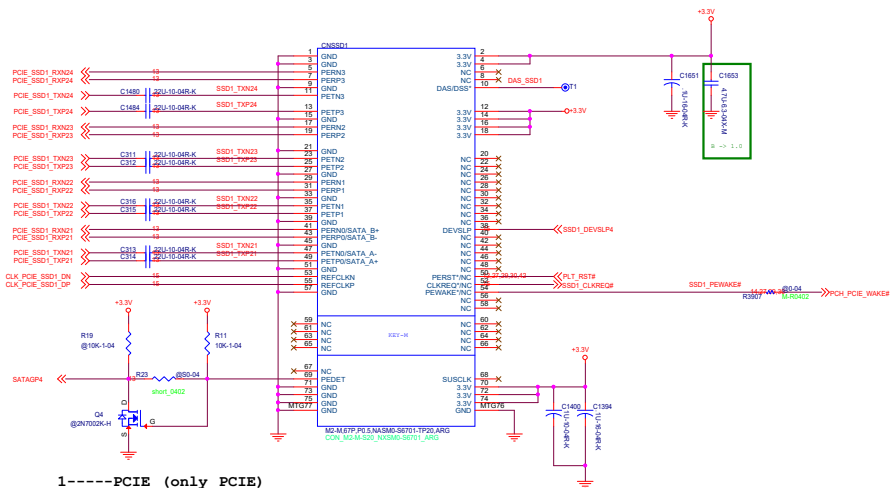


SSD2



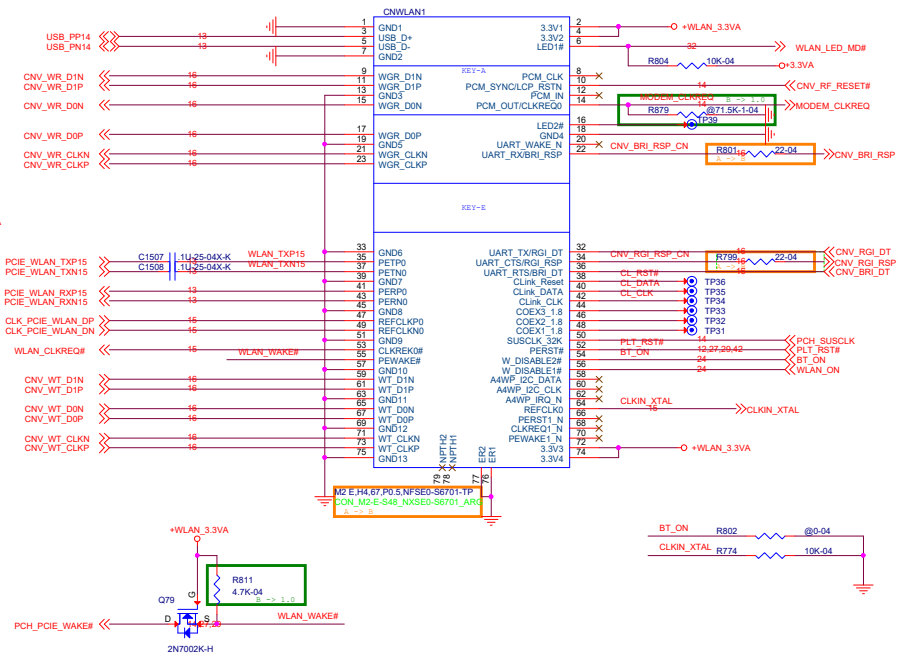
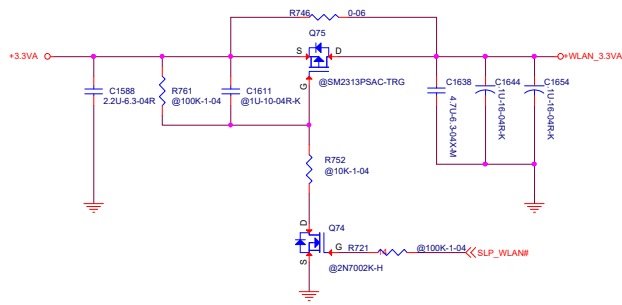
```
0-----SATA
1-----PCIE
```

SSD1

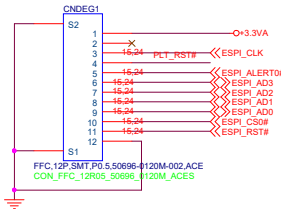


1-----PCIE (only PCIE)

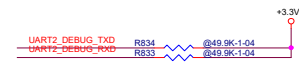
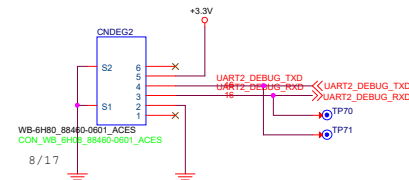
WLAN CONN



ESPI debug port

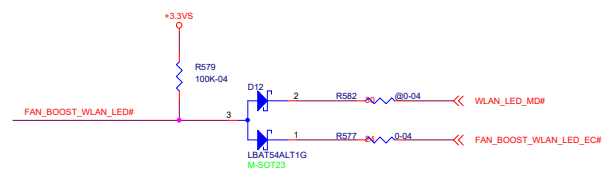
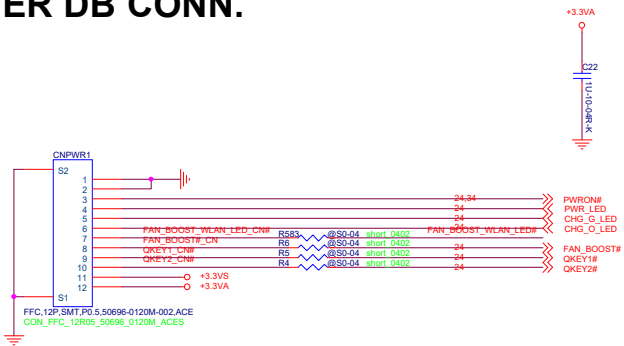


UART debug port

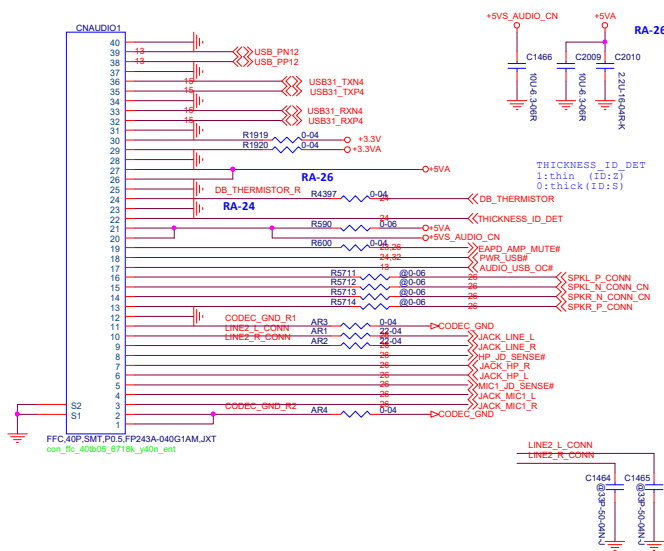


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31_TP/CP/FAN/LB/FP			
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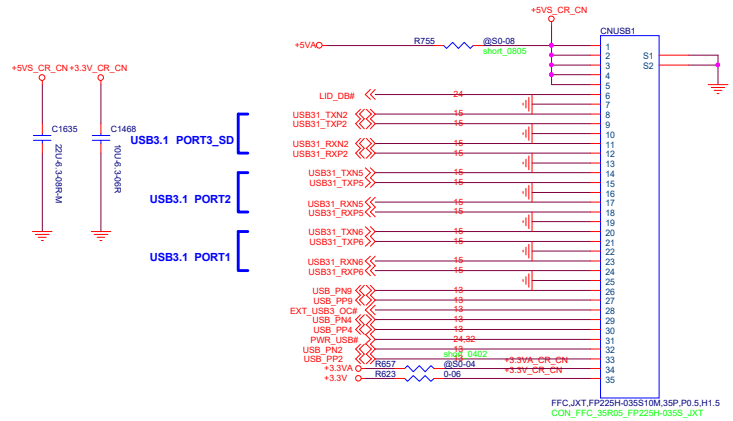
POWER DB CONN.



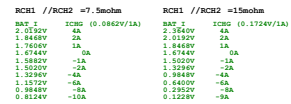
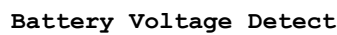
Audio&USB DB CONN.



USB3.0 DB CONN.

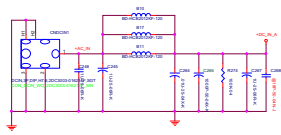


同方国际信息技术有限公司			
Title 32_PWR_DB/USB3.0 DB/Audio DB			
Size	Document Number	GM7MGxx	
Custom		Rev A	
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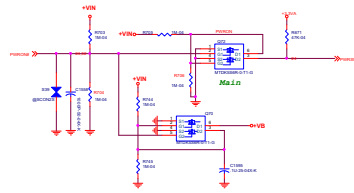
 同方国际信息技术有限公司			
33_BATT IN/CHARGER(BQ24781)			
Size	Document Number	Rev A	
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+DC_IN

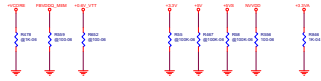


DCDC1000-01
Vout=1.0V
Iout=1.0A
Ripple=10mV
Efficiency=95%
Power=1.0W
Temp=0~100°C

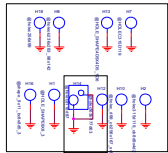
POWER SW



Discharge Resistor



PCB HOLE



WLAN HOLE



THERMAL HOLE



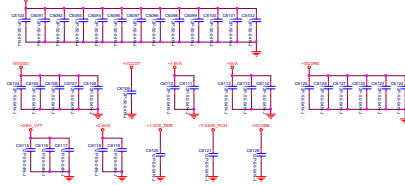
GPU



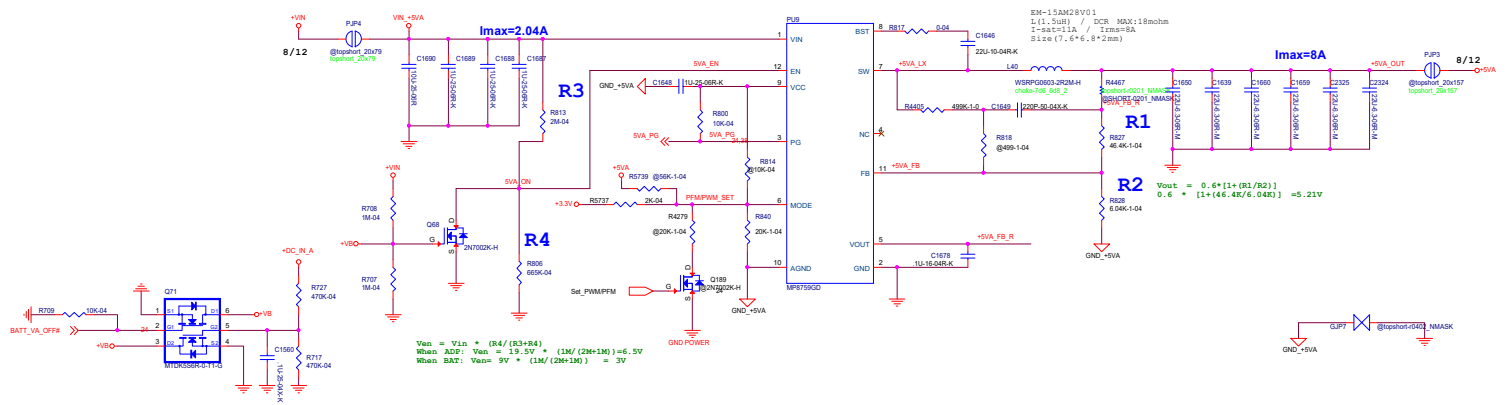
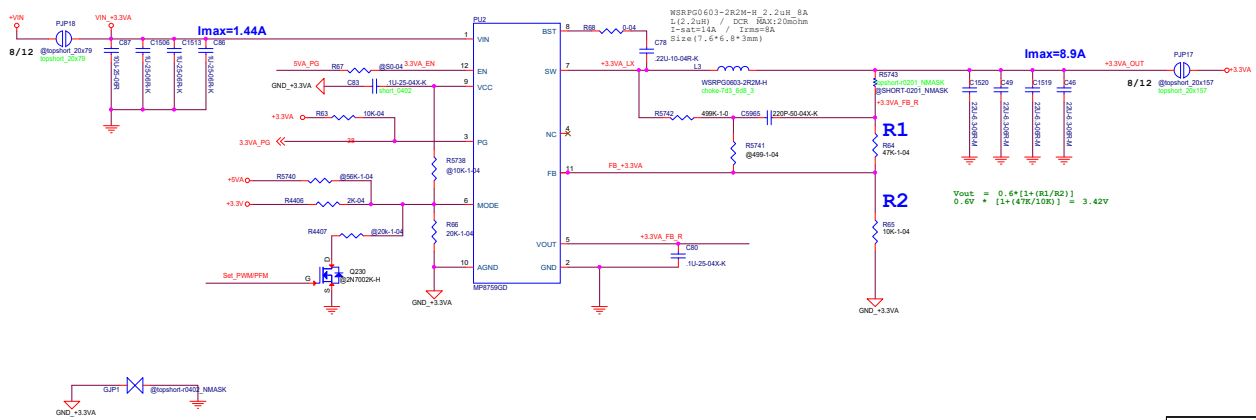
CPU



For 9F solution



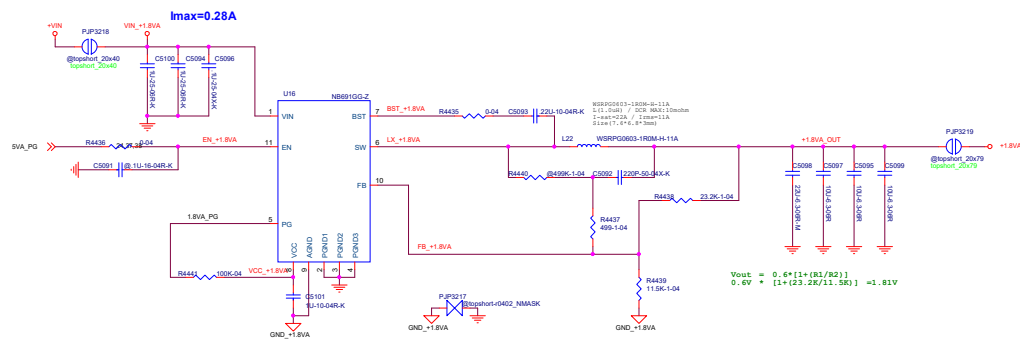


+5VA**+3.3VA**

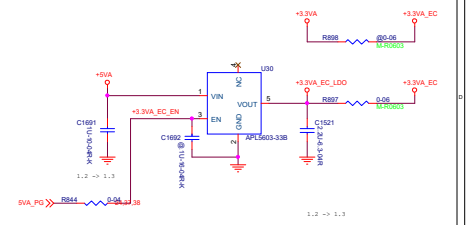
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37_POWER +5VA/+3.3VA	GM7MGxx	A
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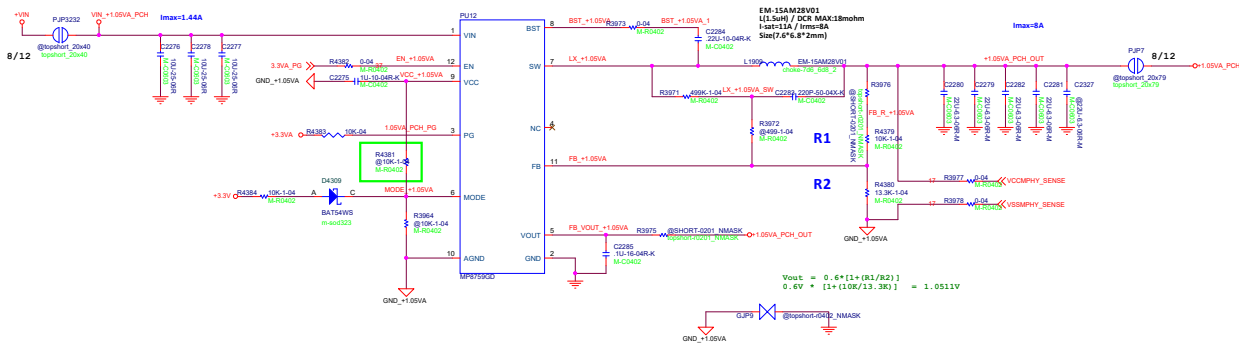
1.8VA Converter



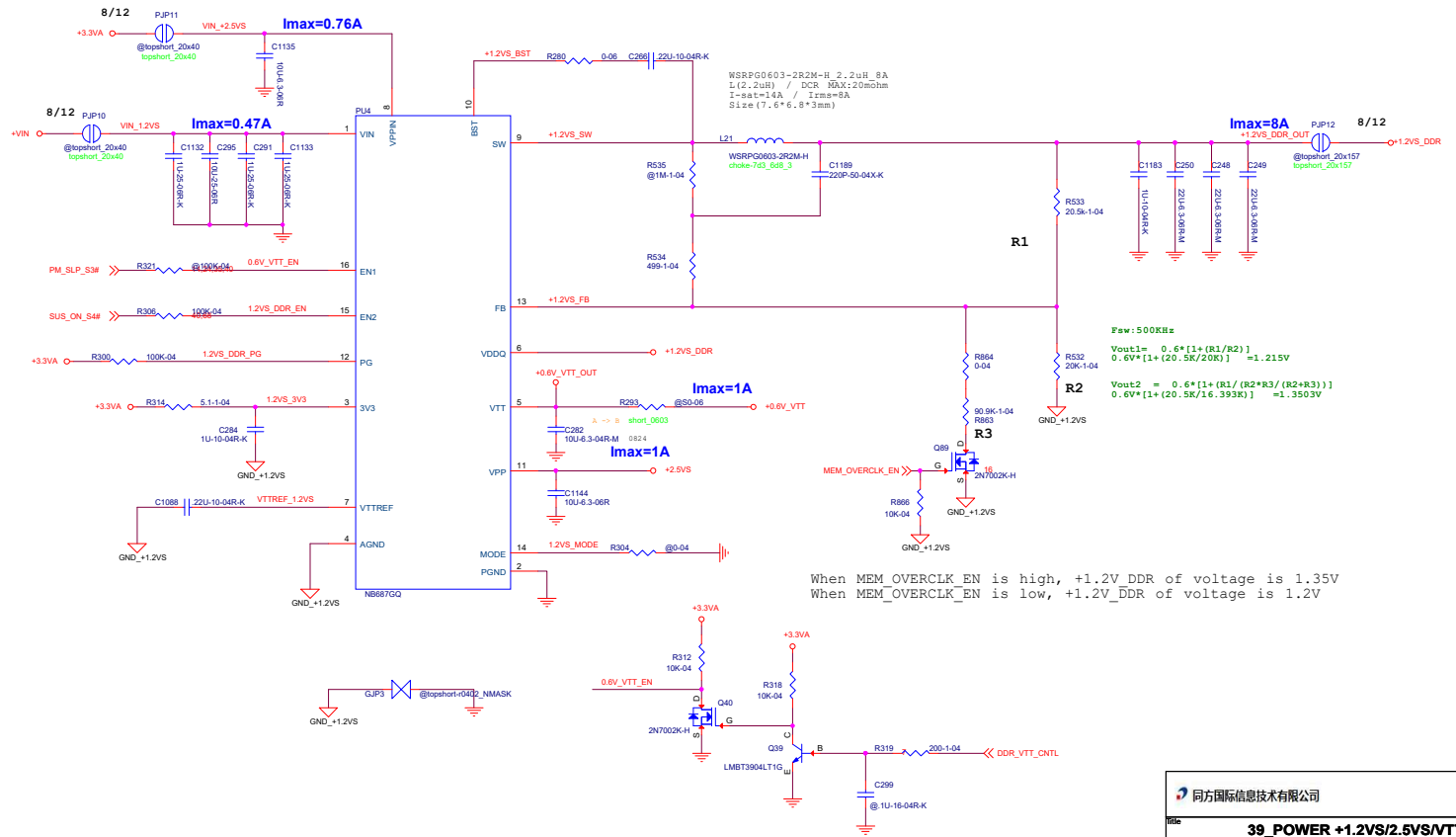
+3.3VA_EC



+1.05VA_PCH

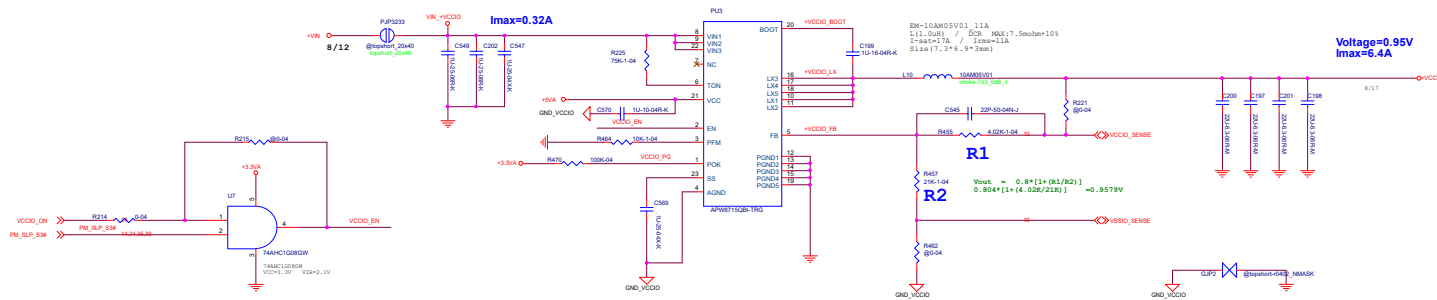


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38_POWER +1.05VA_PCH+3.6_LCD			
Doc	Document	Number	GM7MGxx
Date	Schematic	August 27, 2005	Sheet 35 of 36

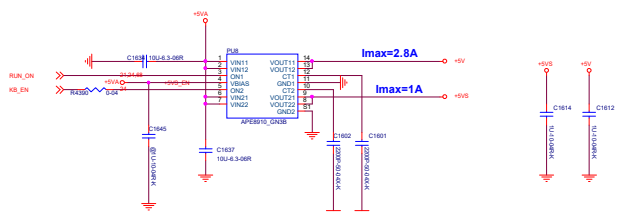
+1.2VS_DDR/+2.5VS/+0.6V_VTT

同方国际信息技术有限公司			
39_POWER +1.2VS/2.5VS/VTT			
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Custom	GM7M9xx		
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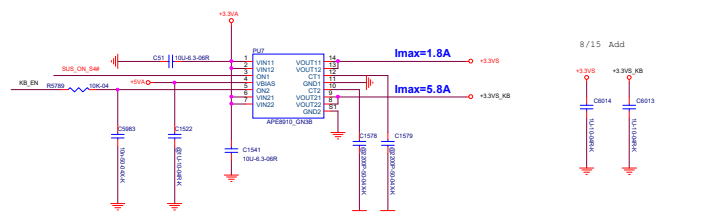
+VCCIO



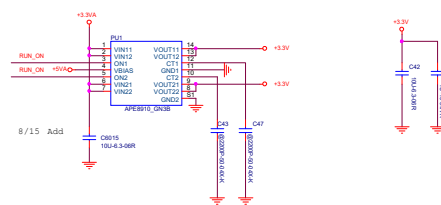
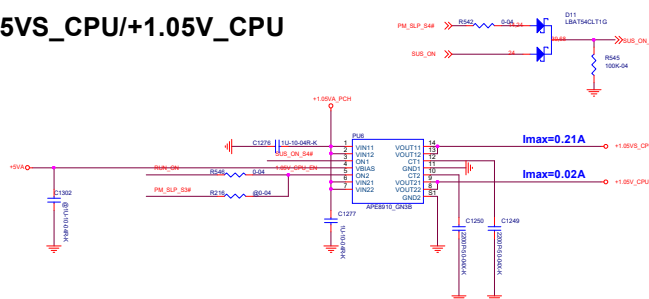
+5VS/+5V



+3.3VS/+3.3V

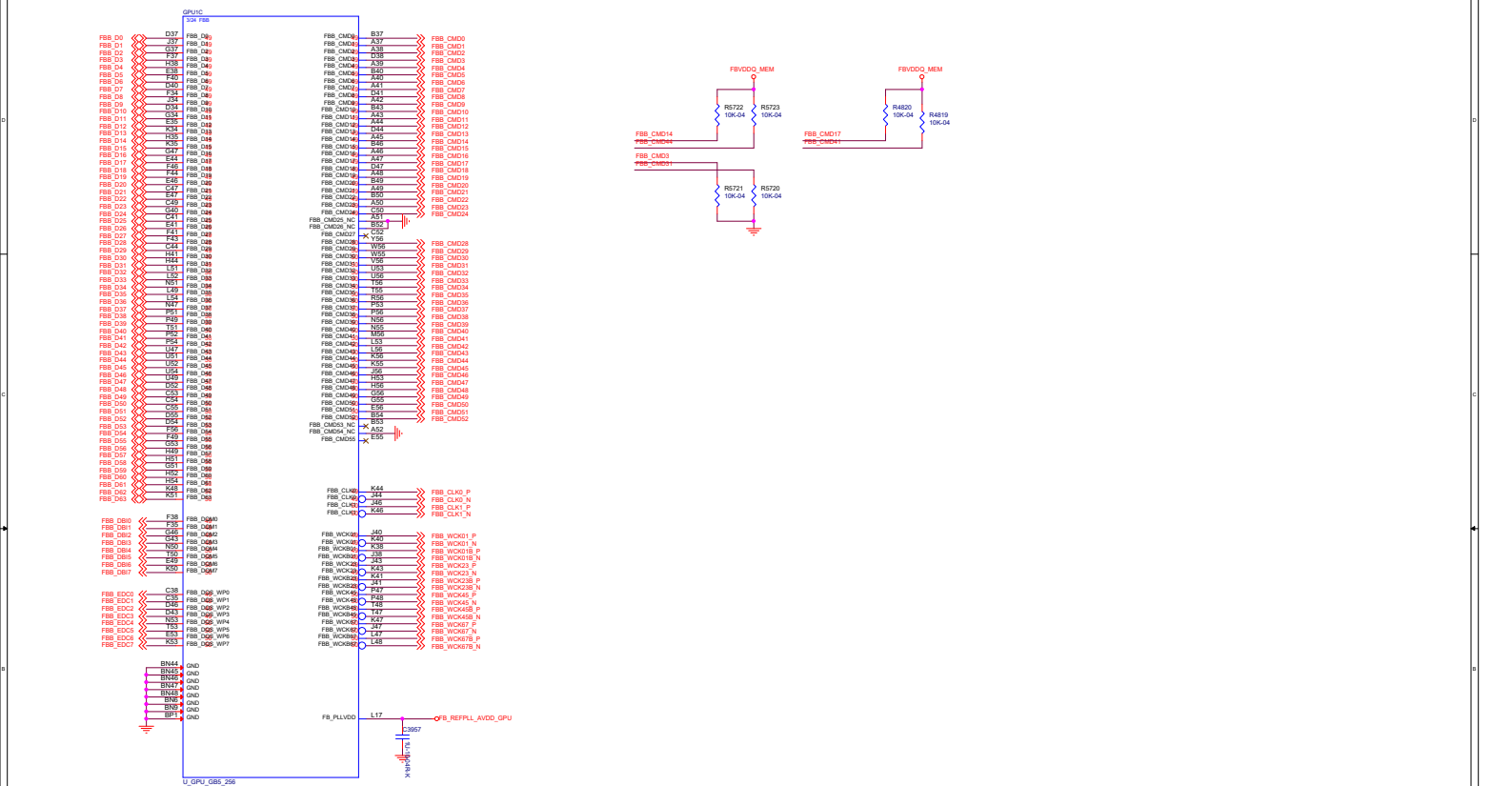


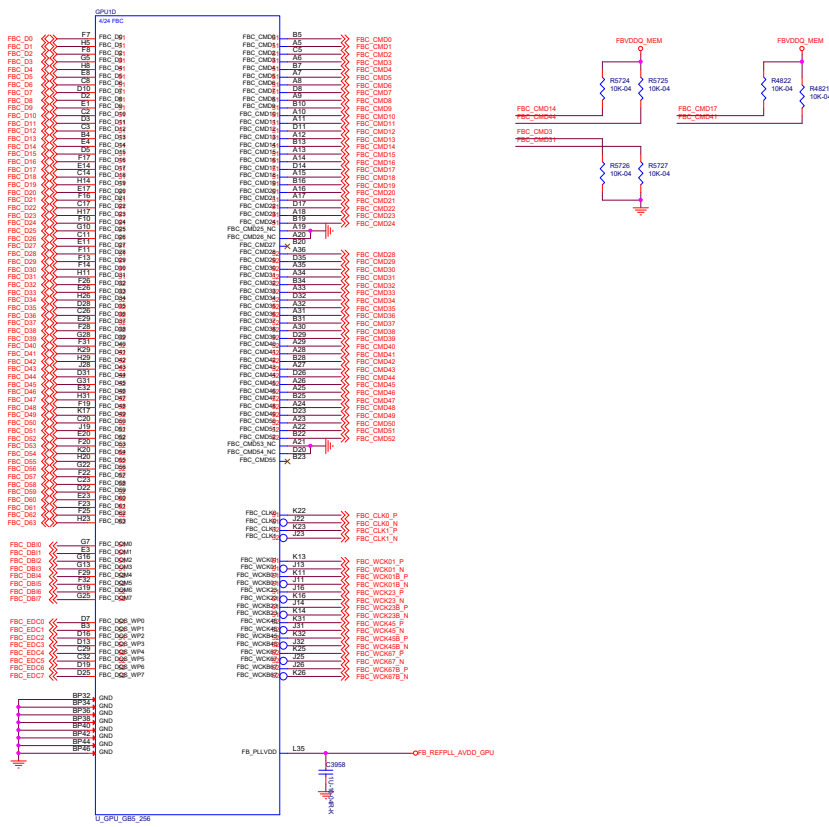
+1.05VS CPU/+1.05V CPU



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Title			
40 POWER +VCCIQ/+VS PWR/+V PWR			
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Printed	Substrate	Assembled	Tested
2000	2000	2000	2000

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Title			
GPU N18E GFX-PCIE			
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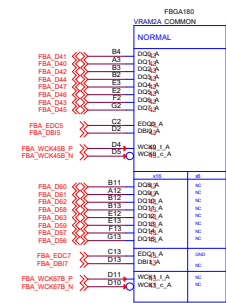




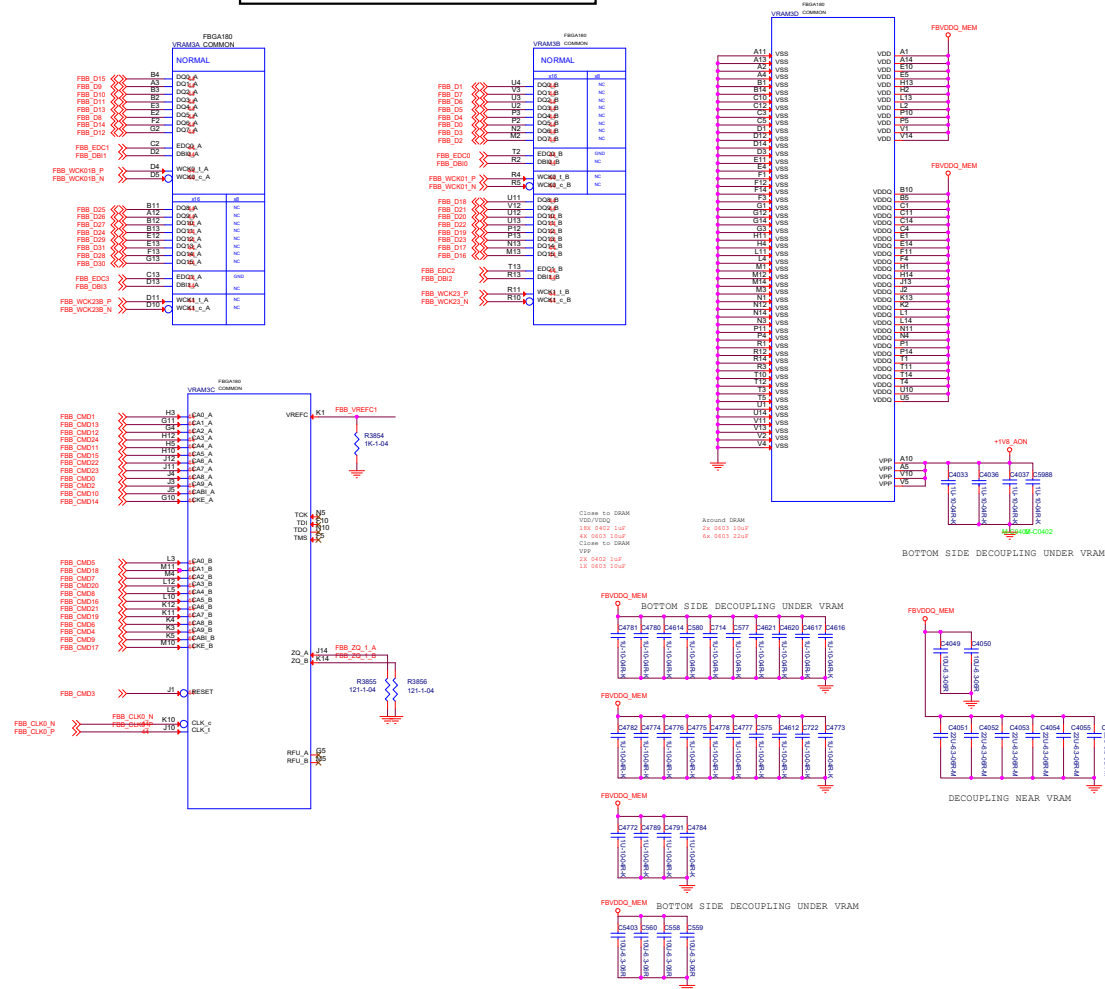
GDDR6: Max
=95 degree

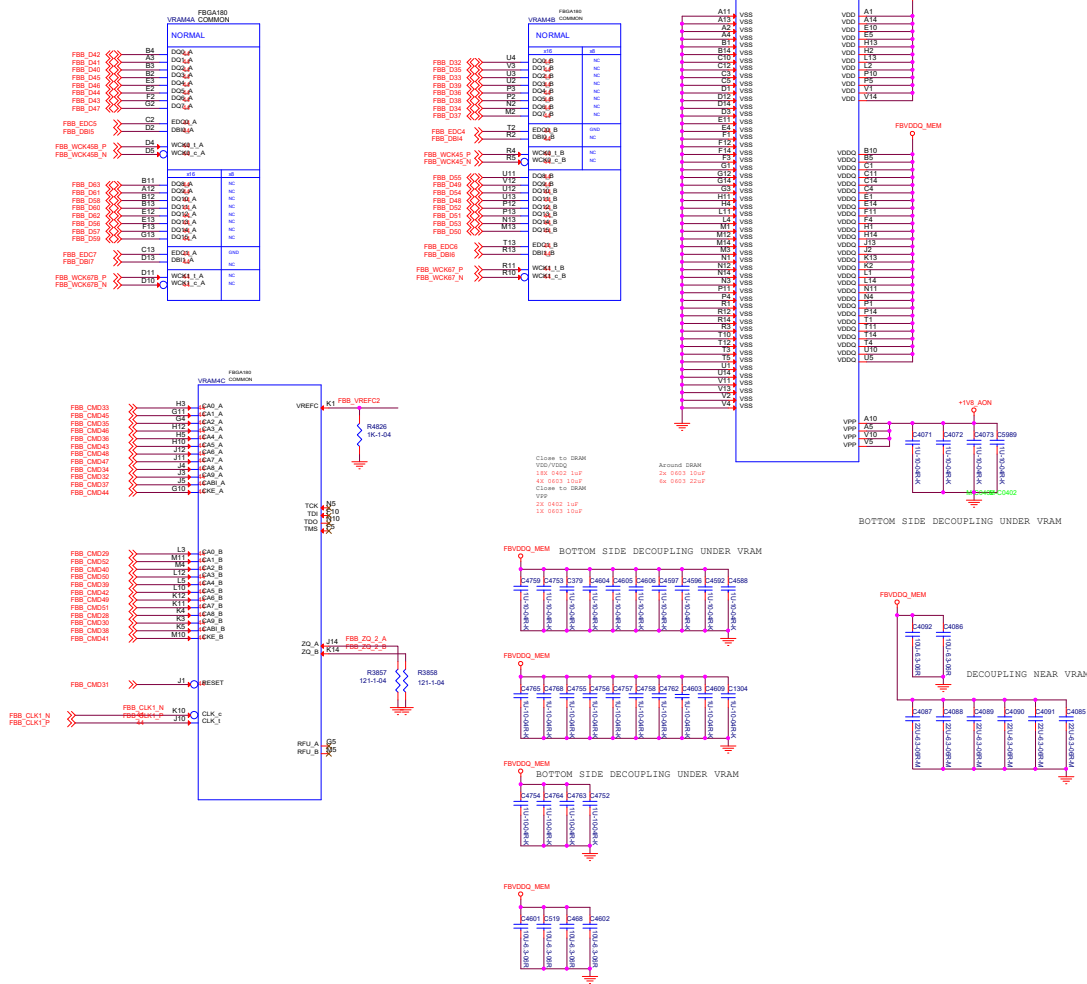


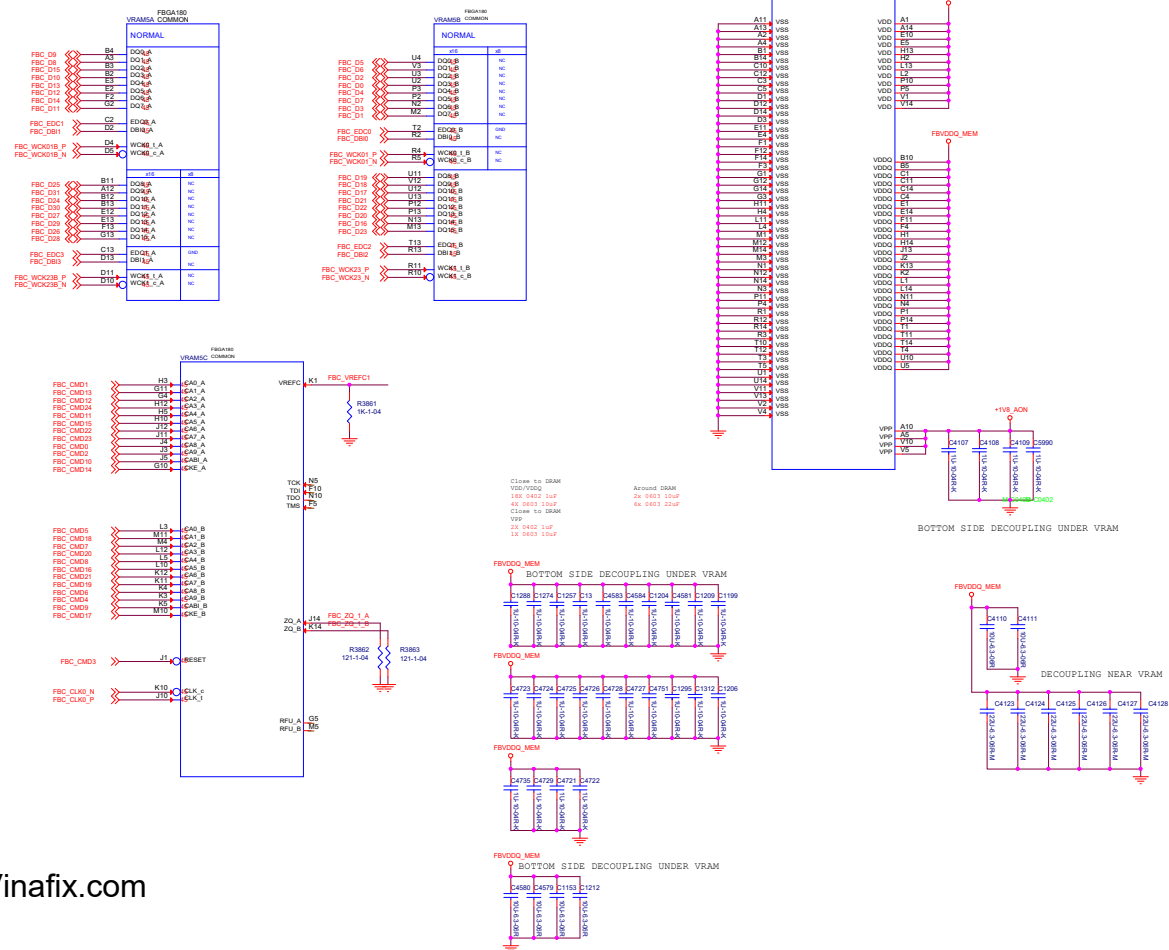
Maximum VRAM case Temp is 85 celcius degree



Maximum VRAM case Temp is 85 celcibus degree

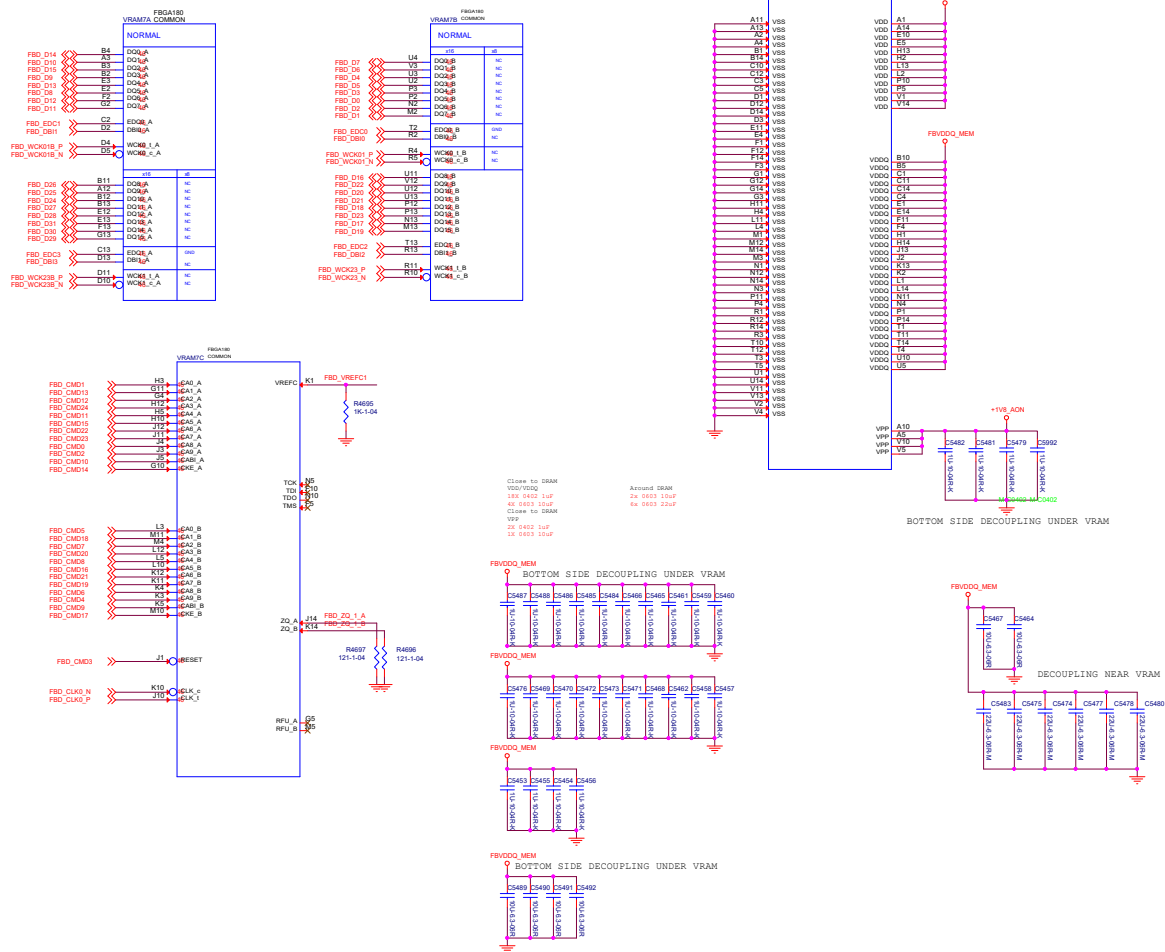


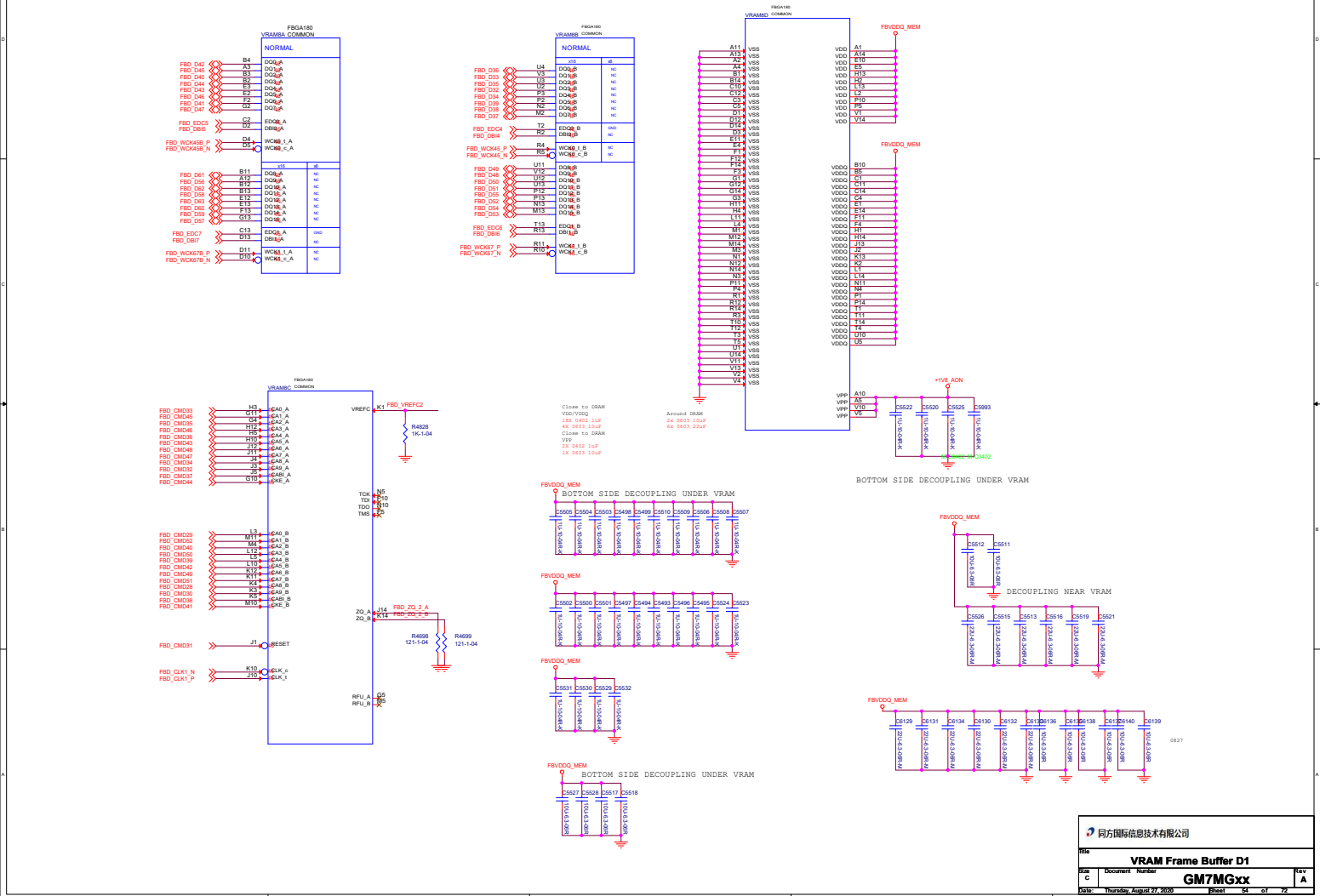




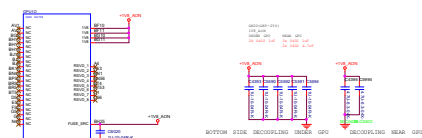
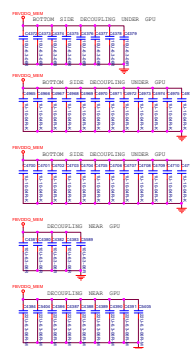
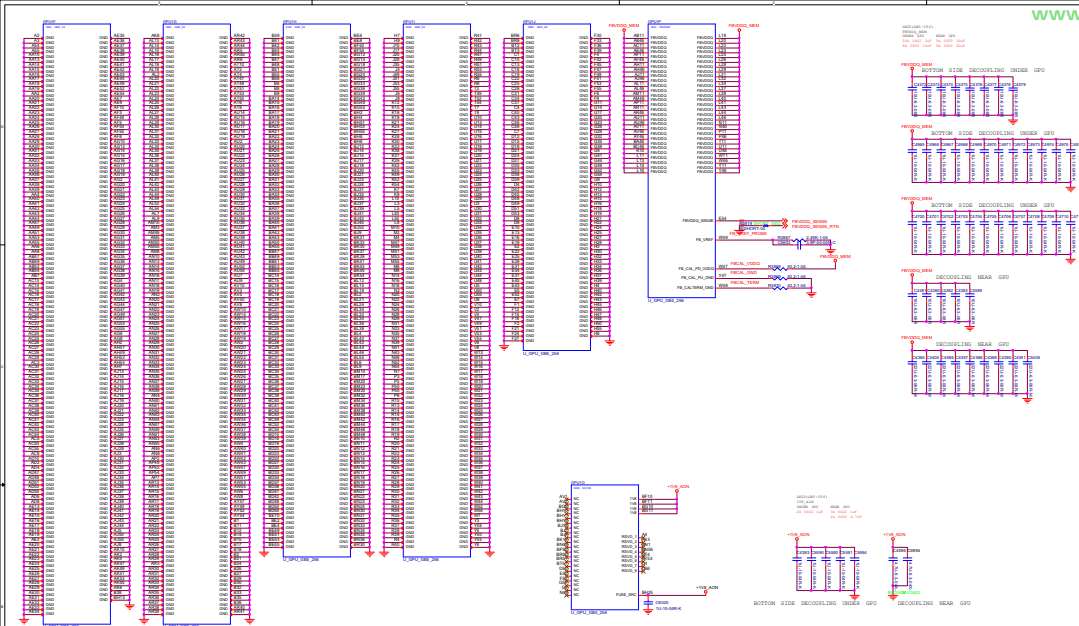
Vinafix.com

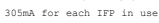












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D

D

C

C

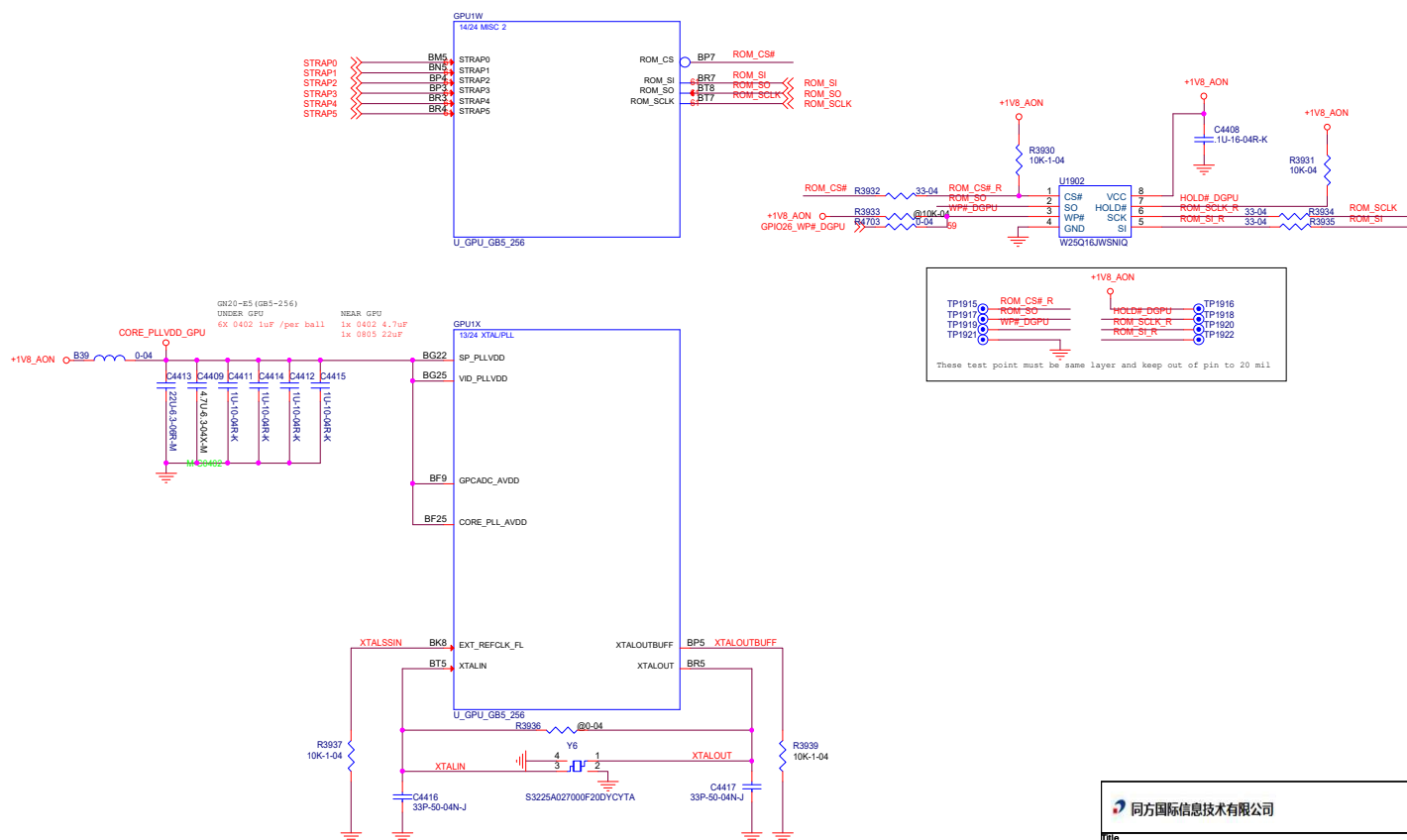
B

B

A

A

 同方国际信息技术有限公司			
Title			
GPU N18E NVLINK			
Size A	Document Number		Rev A
	GM7MGxx		
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GPU N18E BIOS/XTAL			
Size B	Document Number	GM7MGxx	Rev A
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Voltage(V)			
LEVEL	Min	Normal	Max
H	1.5	1.8	1.854
M	0.5	0.9	1.3
L	0	0	0.3
Invalid	1.3V<pin voltage<1.5V		
	0.3V<pin voltage<0.5V		

GN20-E5 GDDR6							
Density	Vendor	Part Number	Strap	Strap 2	Strap 1	Strap 0	
8Gb	Samsung	K4Z80325BC-HC14 C-die	0X0	L	L	L	
8Gb	Micron	MT61K256M32JE-14:A A-die	0X1	L	L	H	
8Gb	Hynix	H56C8H24AIR-S2C A-die	0X2	L	H	L	

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Strap5,4,3 LLH				
SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
0	0	0	1	

Strap5,4,3 HLH				
SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
0	1	0	1	

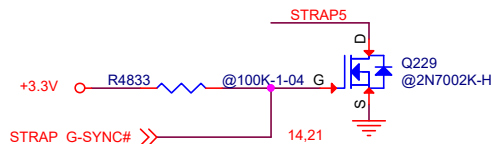
1:SMB_ALT_ADDR dual GPU alternate
0:SMB_ALT_ADDR single GPU

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG reduced signal amplitude
0:PCIE_CFG normal signal swing

1:VGA_DEVICE class code 300
0:VGA_DEVICE class code 302

STRAP0
STRAP1
STRAP2
STRAP3
STRAP4
STRAP5



FS OVERT			
FUNCTION	ROM_SO	ROM_SI	ROM_SCLK
disable	L	L	L
enable	L	L	H

ROM_SI
ROM_SO
ROM_SCLK

ROM_SI
ROM_SO
ROM_SCLK

+1V8_AON

+1V8_AON

60
60
60
60
60
60

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Title

GPU N18E STRAP

Size

Document Number

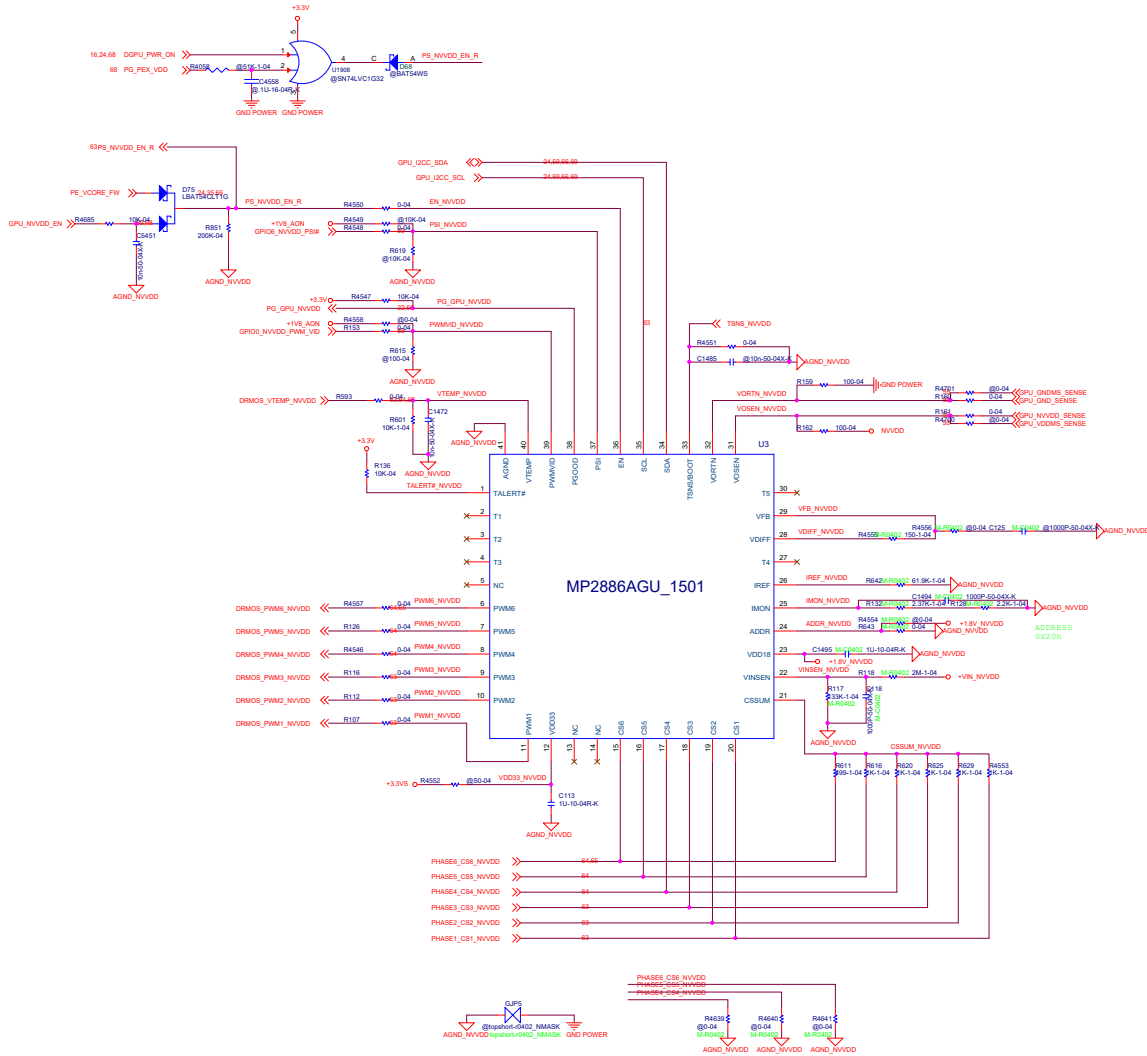
GM7MGxx

Rev

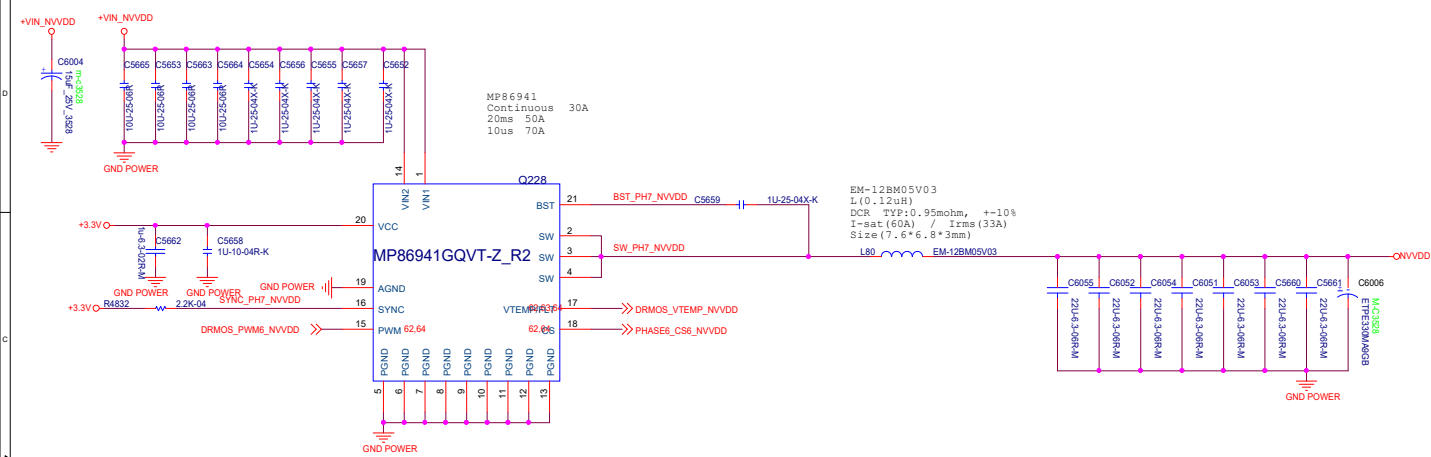
A

Date: Saturday, August 22, 2020

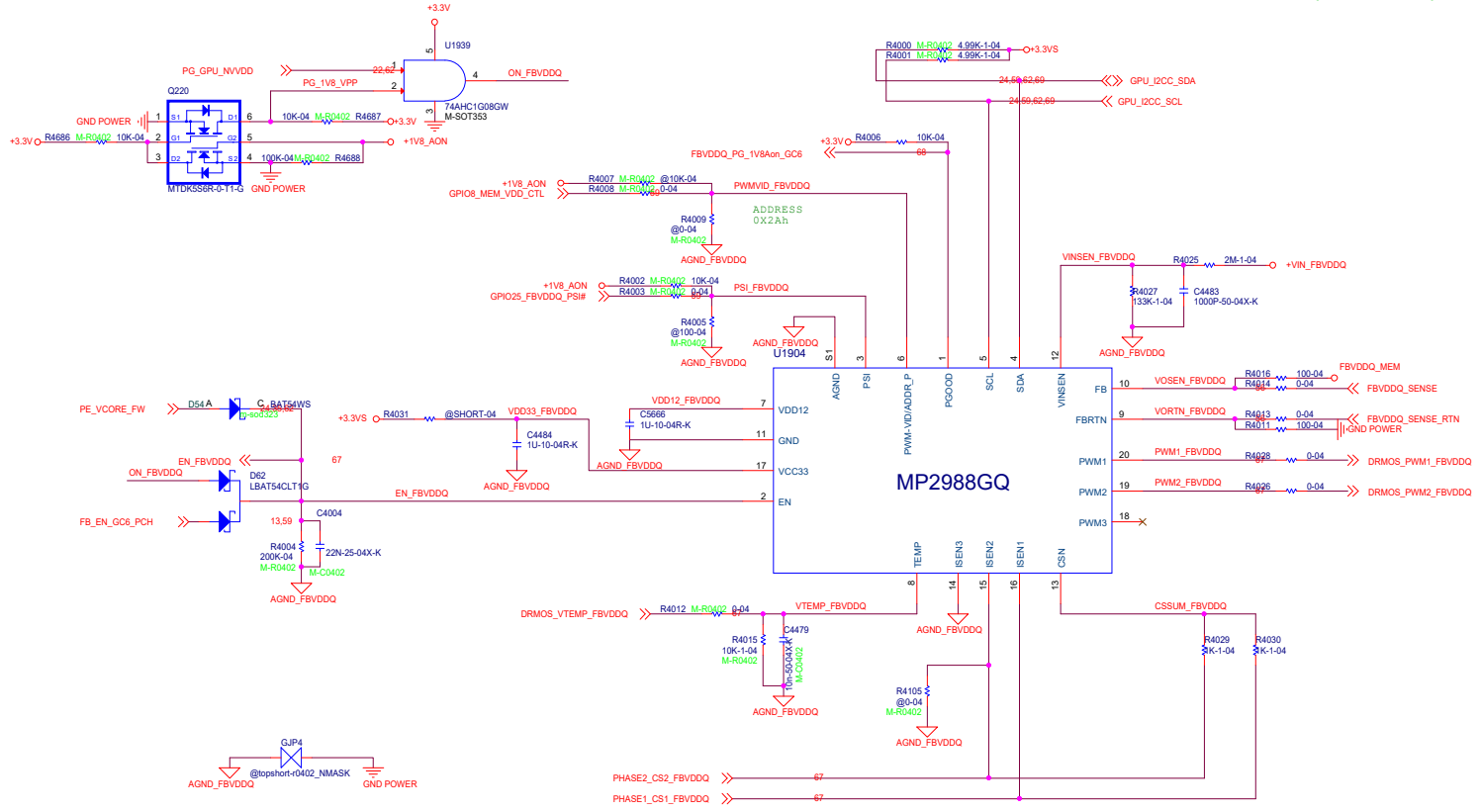
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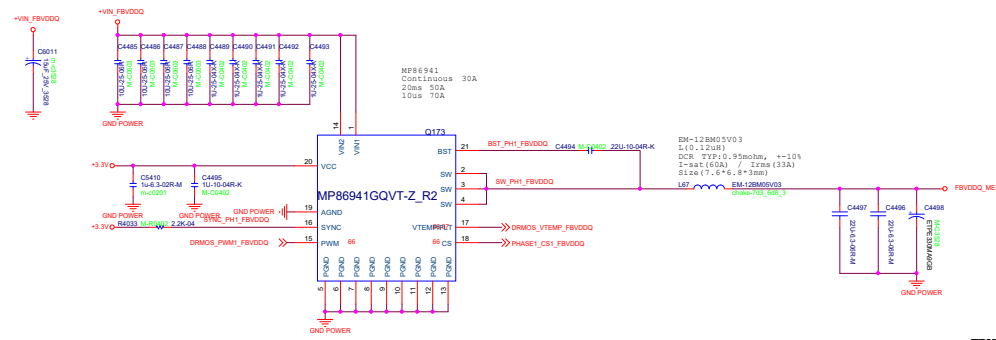
同方国际信息技术有限公司			
Title: POWER N18E NVDD CONTROLLER			
Rev: C	Document: Number	GM7MGxx	Rev: A
Date: Monday, August 24, 2020	Sheet: 10	of: 12	



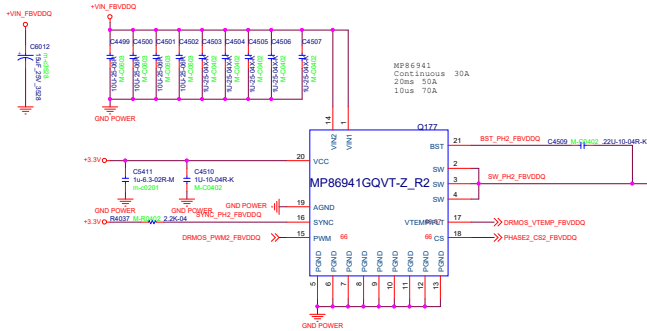
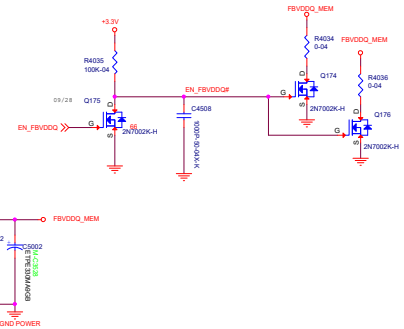
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FBVDDQ NEM 1.2V/1.25V/1.35V
GN20-E5 ICCMAX:26A
GN20-E5 IPEAK(6us):30A
GN20-E7 ICCMAX:36A
GN20-E7 IPEAK(6us):41A
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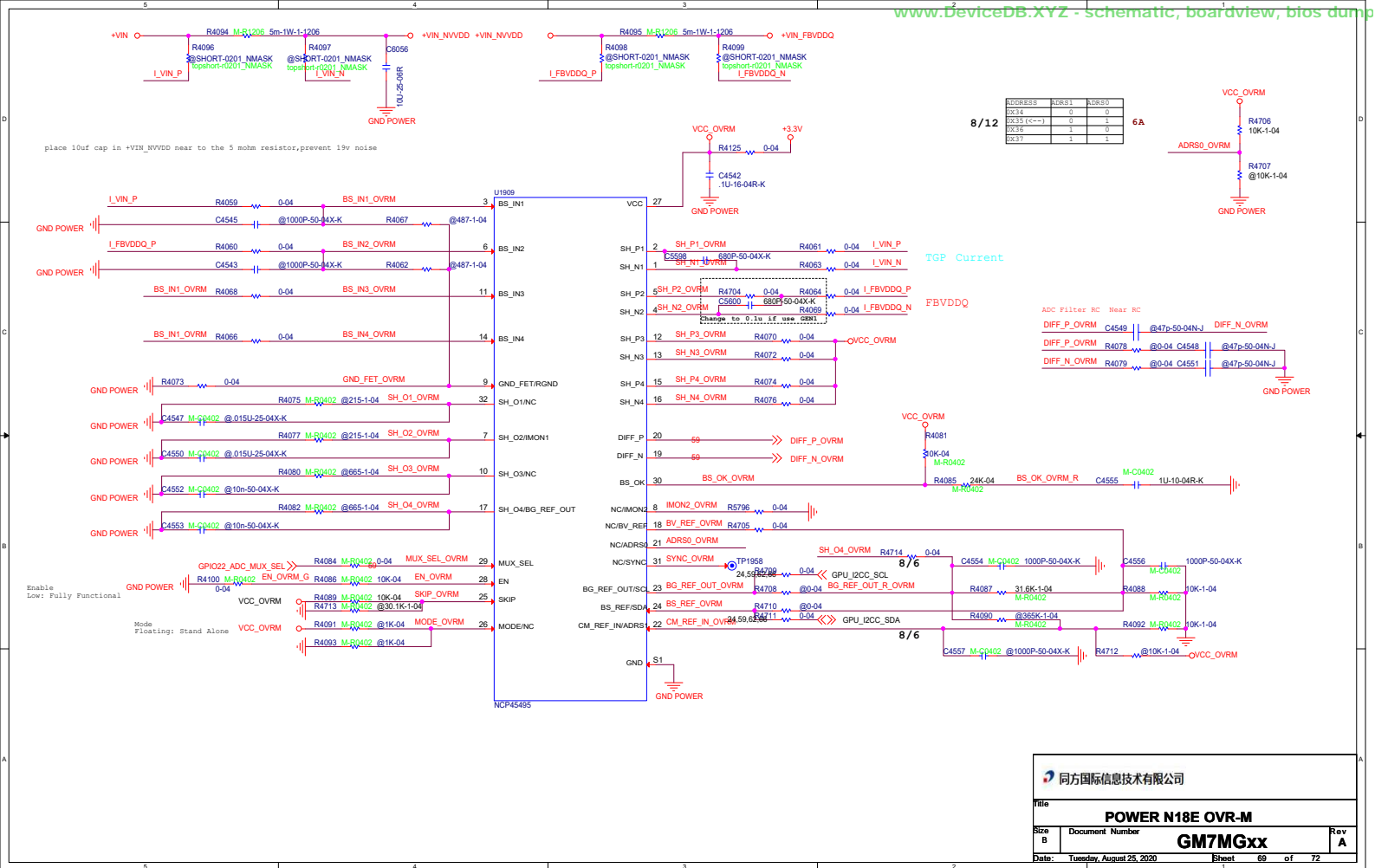


FBVDDQ_MEM_Discharge



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POWER N18E FBVDDQ 2PHASE			
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POWER N18E PEX_VDD/1V8_AON			
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No.	Modify Item	Modify Details	Schematic/Layout/BOM Change	Page
1	B1-1 Add capacitor for D05 AUXPANEL solved non-D05 LG panel no display	C8037,C8038	Schematic&BOM&Layout	27
2	B1-2 Change R733 value for DB thermistor	R733(10K to 47K)	Schematic&BOM	36
3	B1-3 Change R3661 value	R3661(47K to 10K)	Schematic&BOM	36
4	B1-4 Changed power plane V16_AON to +3.3V_LCD for pull up	R4364,R4365	Layout	64
5	B1-5 Changed C443 value for ME interference	C433(bx EEEH61E330L)	BOM	46
6	B1-6 Changed U1908 PCB footprint	U1908	Schematic&Layout	72

1. Add jumper for power
2. C1333 stuff
3. R1008 R1009 should support R100C - pending
4. Modify IIC address
5. R5744 (Stub to 100K)
6. Add C8011&C8012
7. Del 100K_W7701 (N2440)
8. U1908&U1909 exchanged Pin
9. Changed R1008&R1009 PCB footprint
10. Del R200316
11. Add media_upgrade_nomenclature
12. Modify CPU power V16 input resistance stuff/default
13. Add New input output manual 6

14. Del C8030
15. Add C8031 to 100
16. Change V16_W7701 (N2440)
17. Change C8037,C8038, C1 10 0 10 100 0V
18. Change C8033 C8035 value 4.7K to 2.2 K page 39
19. pull down C8037 C8035 V value 1V1 to 0V2 page 36
20. Change C8037 value 10K to 0 - commented page 36
21. remove pull up C8042 page 41
22. delete C8036,C8038,C8039,del
23. Add media_upgrade (C8037,C8035) page 41&42
24. pull 2 pull up 10 K&1K -commented page 39
25. delete C8037, C8038,C8039,C8042 page 39
26. delete stuff C8039 page 39
27. Add pin_V16_W7701 and C8036,C8037,C8038,C8039,C8042 page 40
28. Add C8036,C8037,C8038,C8039,C8042 page 40
29. Add C8036,C8037,C8038,C8039,C8042 page 40
30. delete C8037,C8038,C8039,C8042 page 40
31. Add C8037,C8038,C8039,C8042 page 40
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